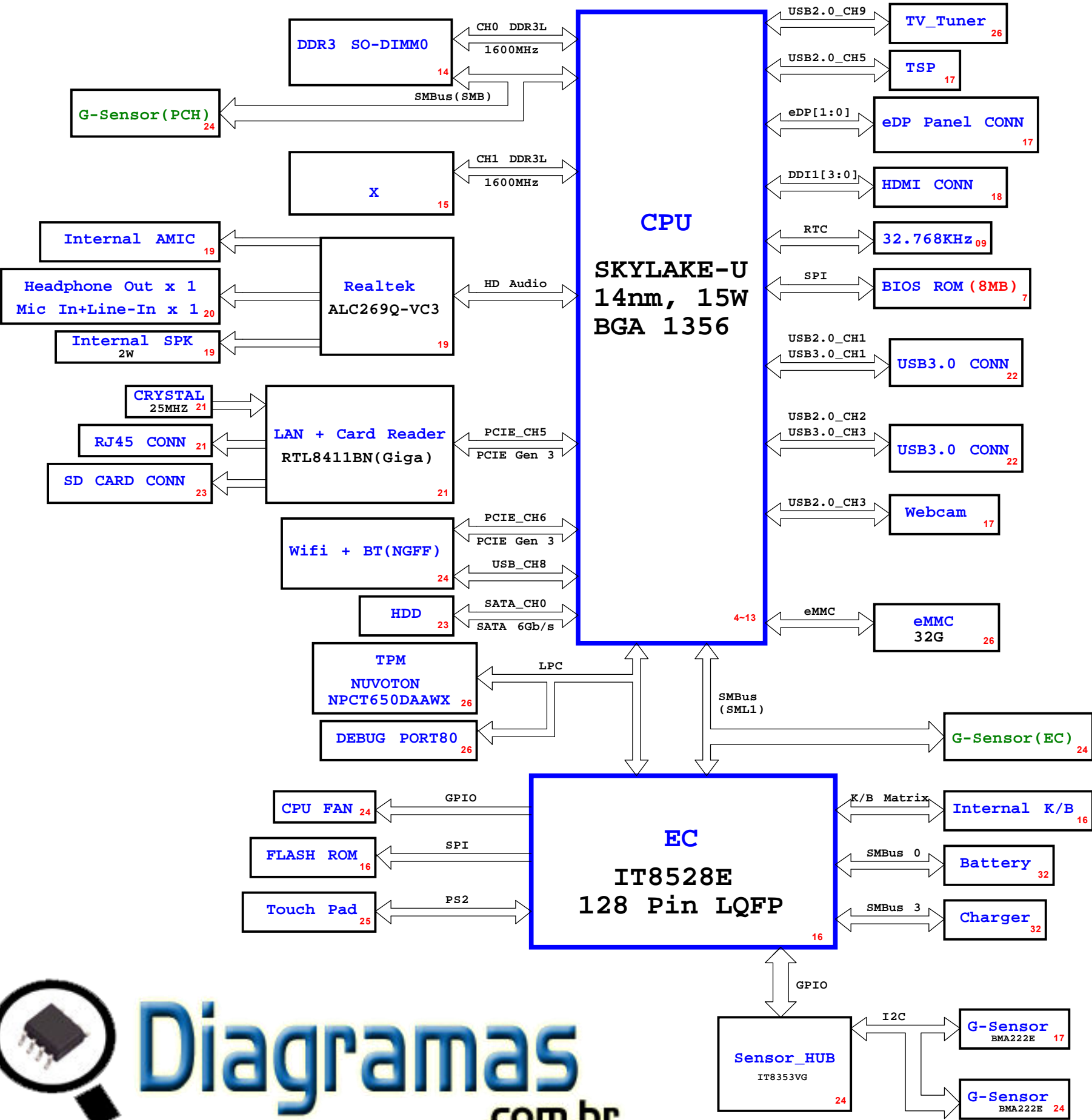
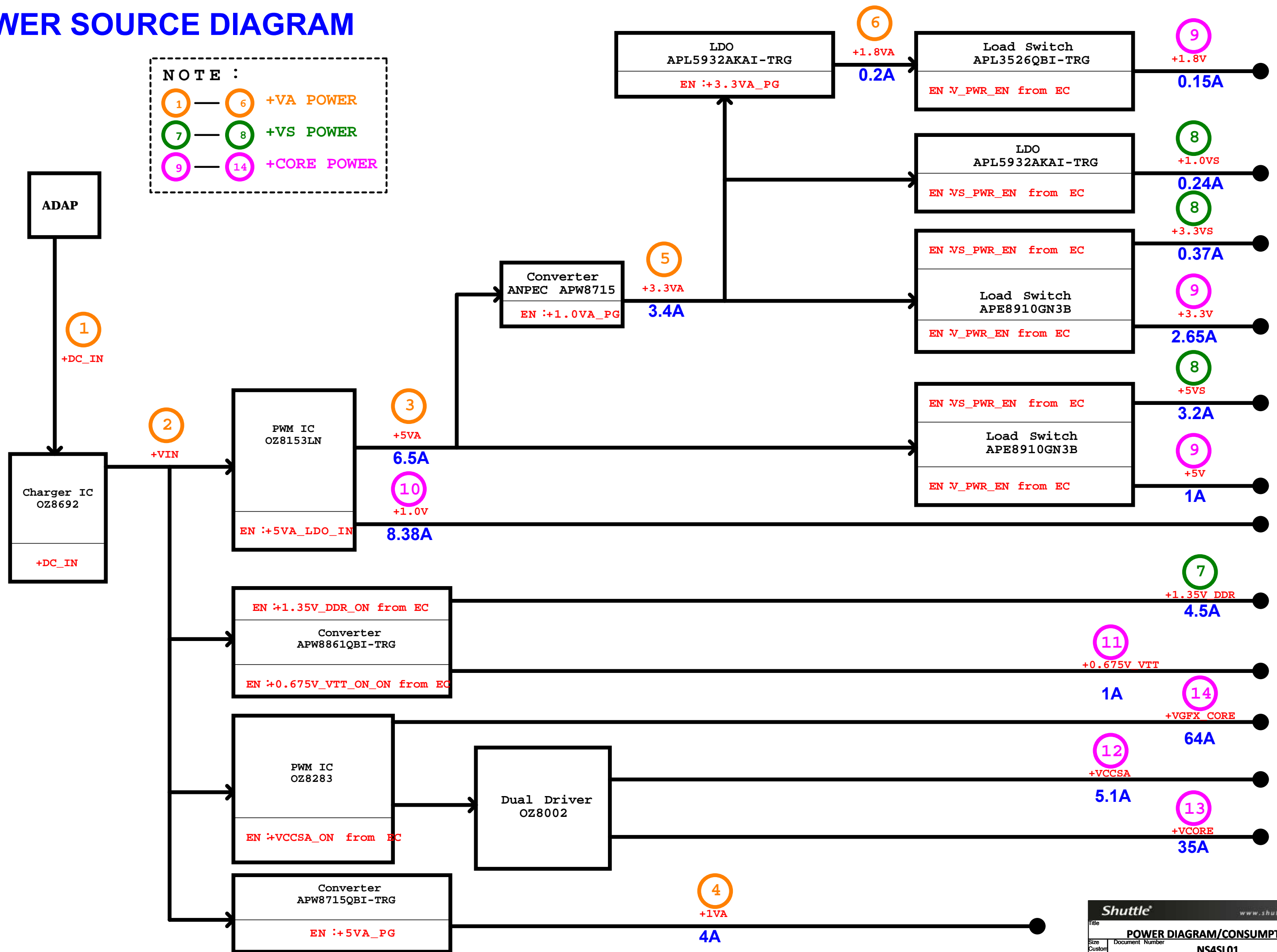


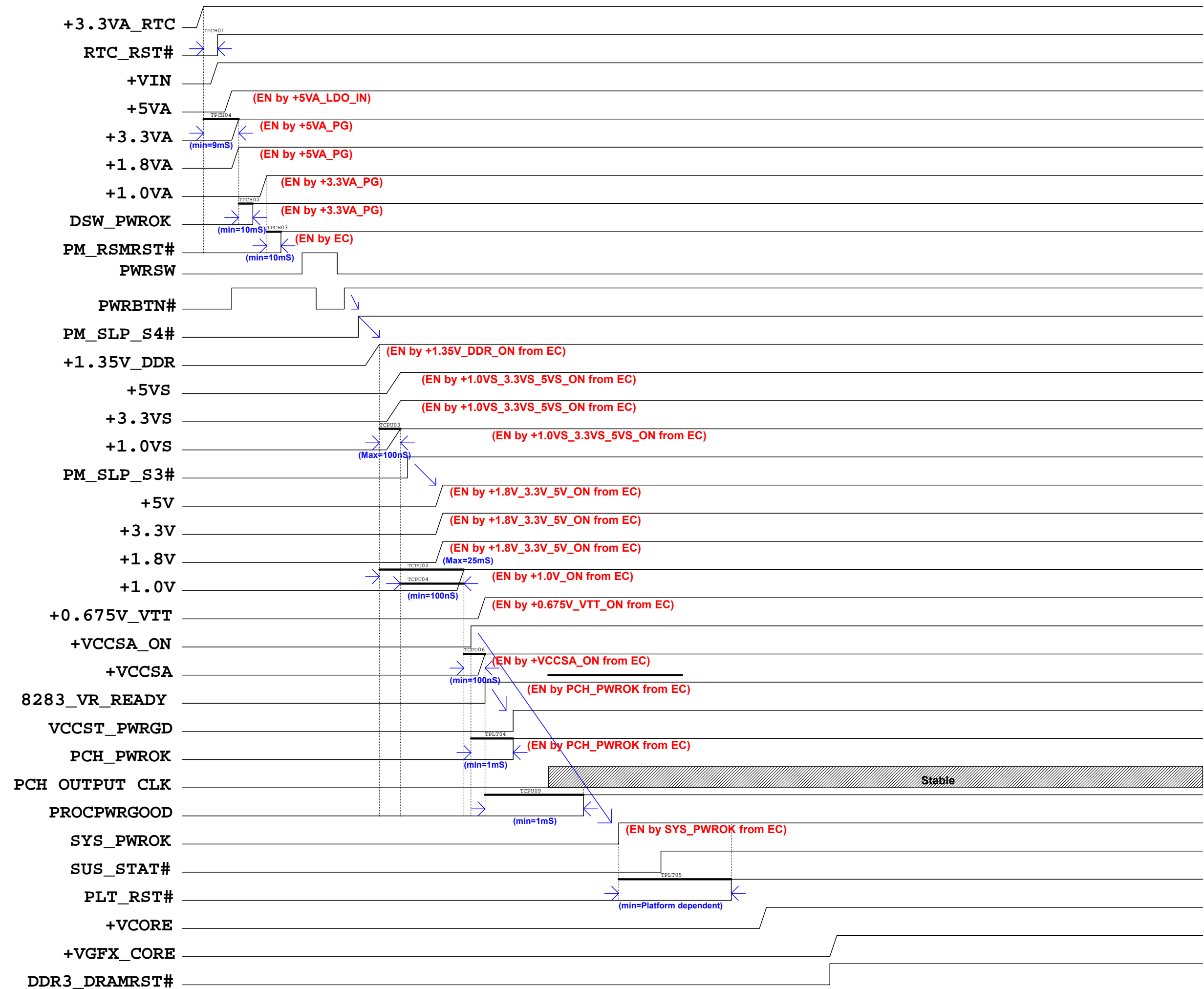
# NS4SL01\_Block\_Diagram

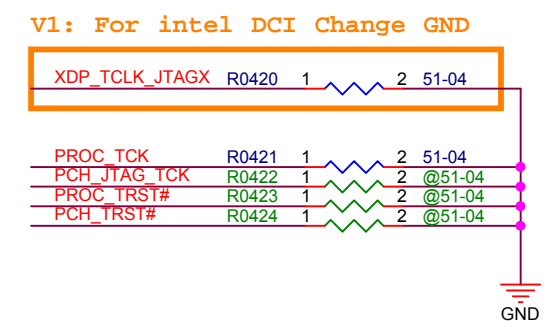
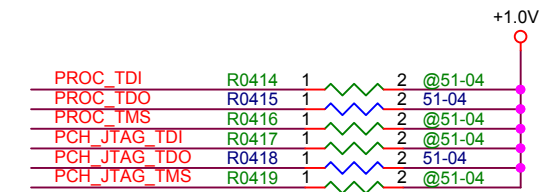
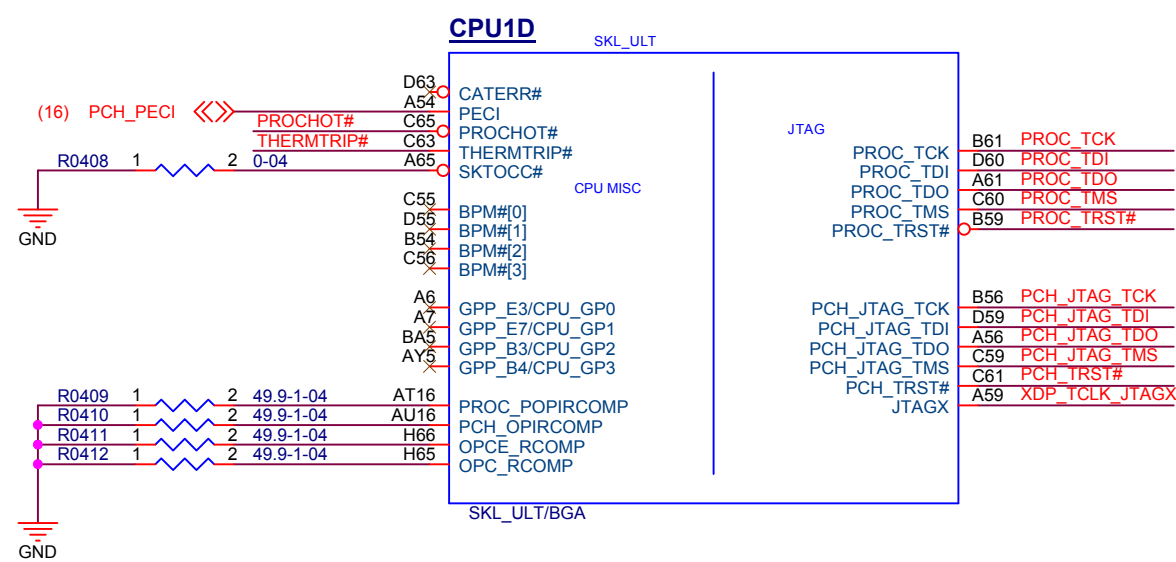
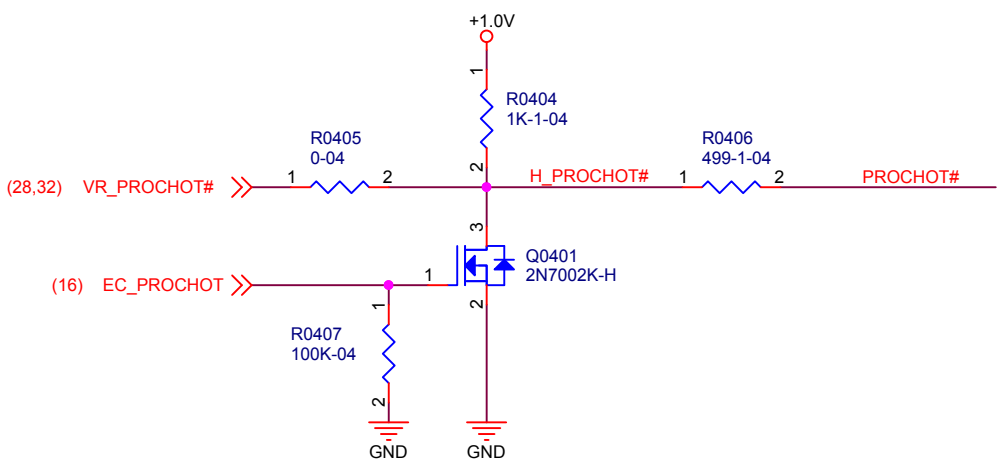
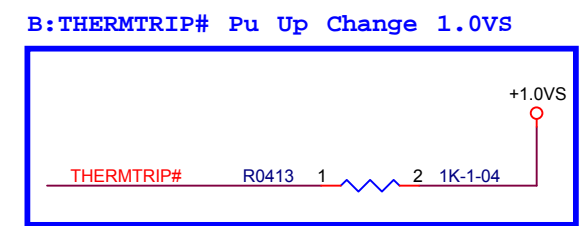
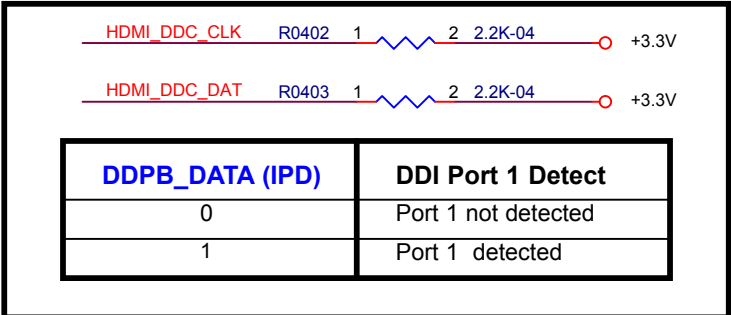
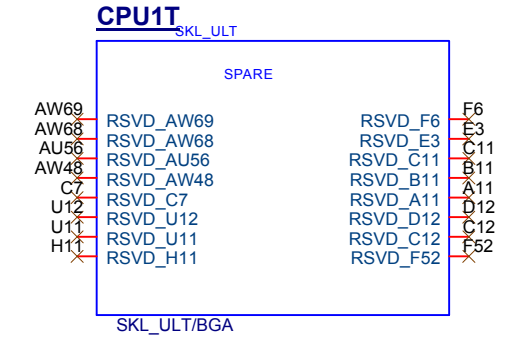
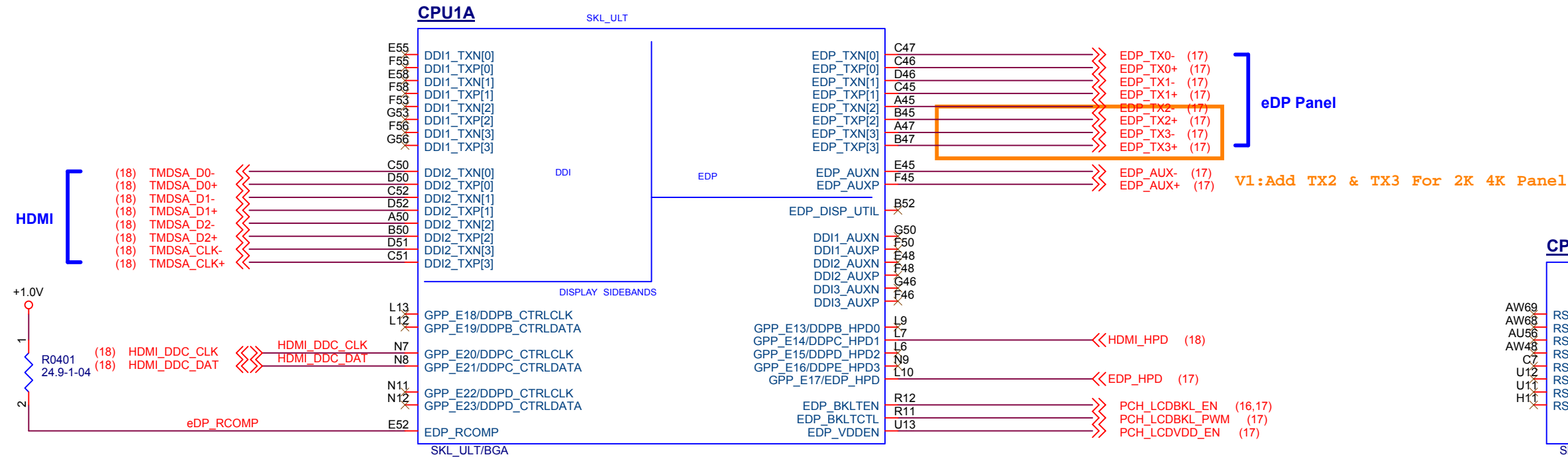


## POWER SOURCE DIAGRAM



# POWER ON SEQUENCE

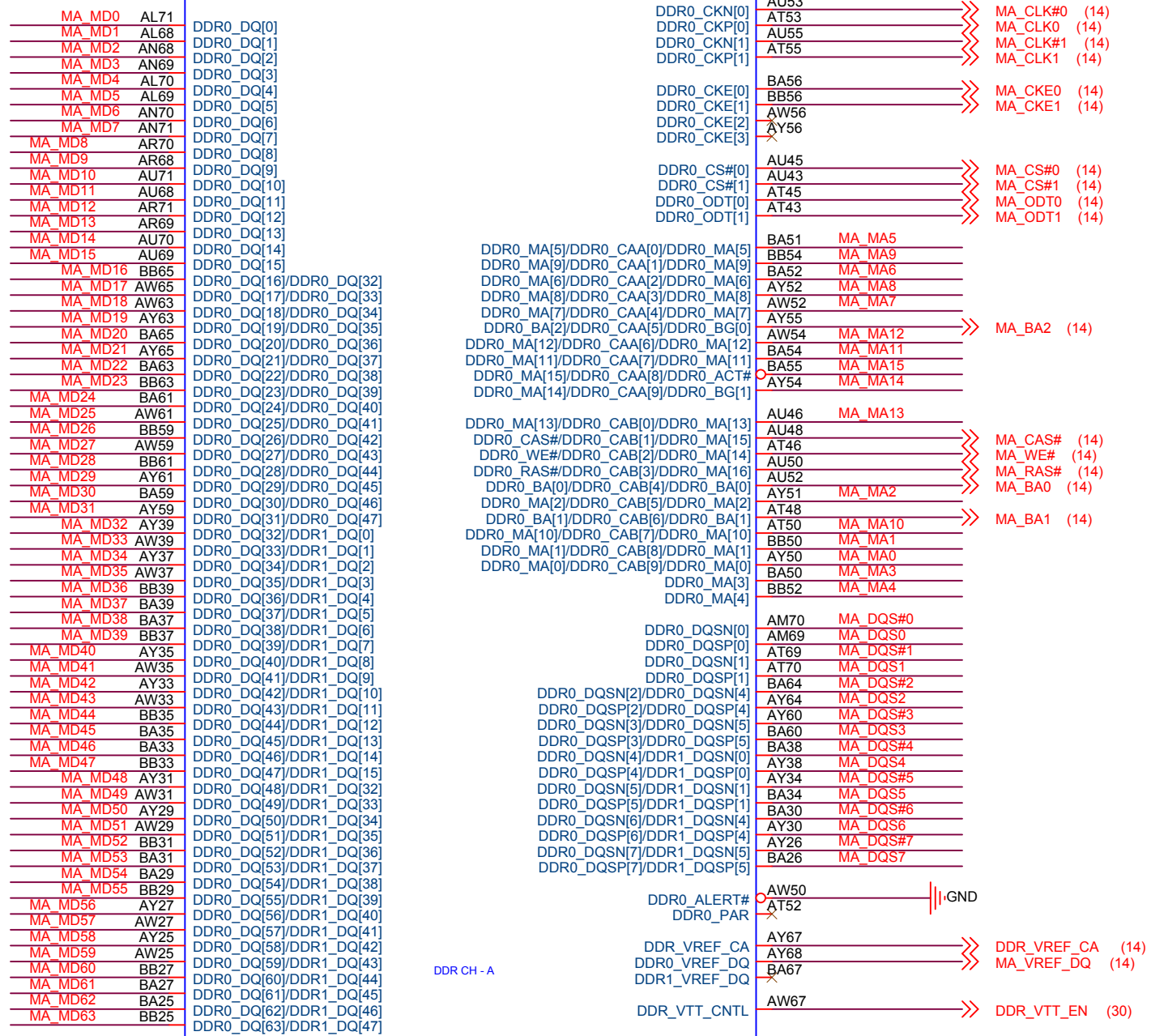






### CPU1B

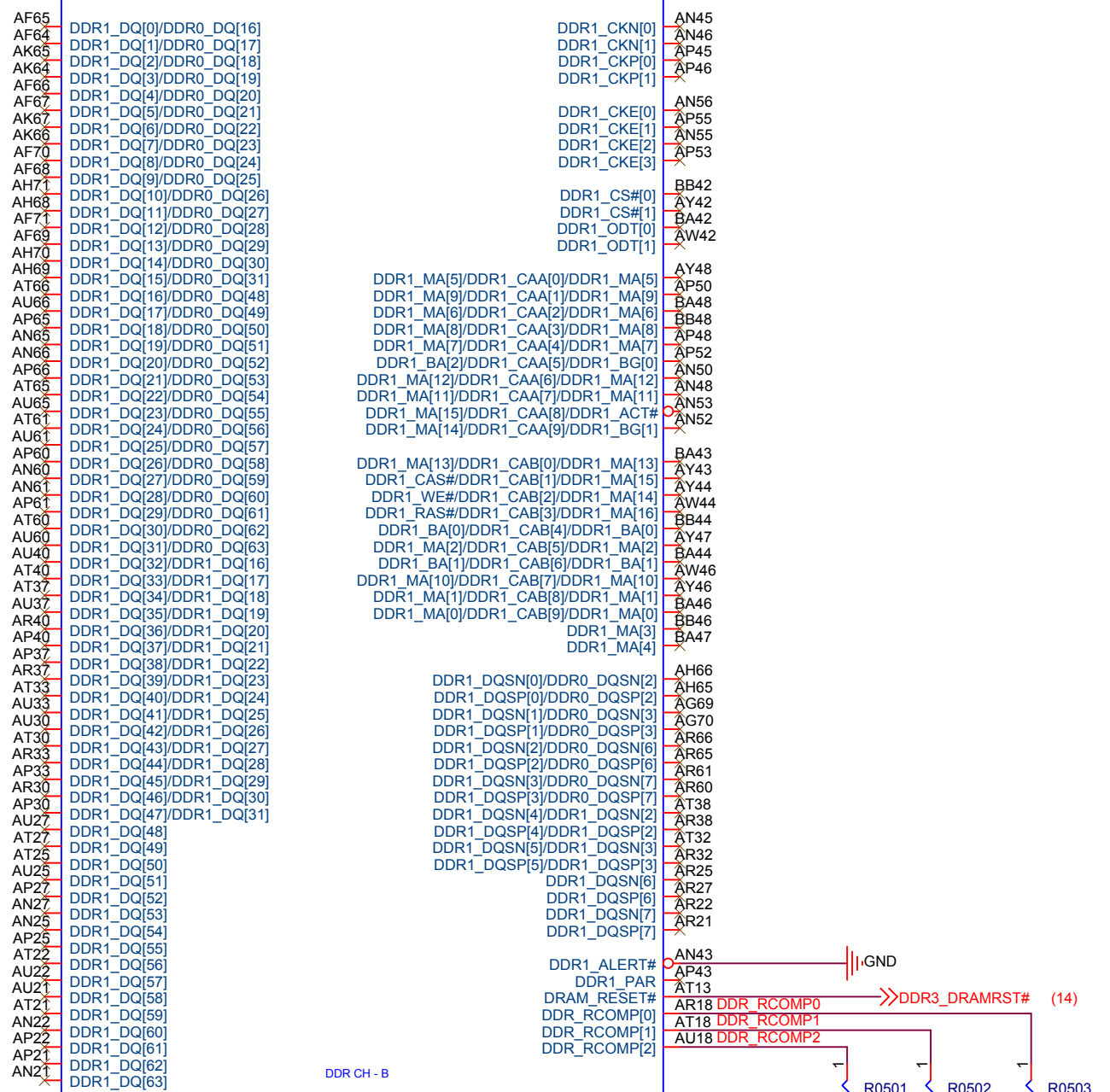
SKL\_ULT



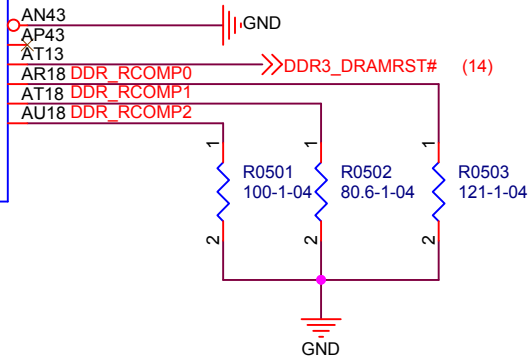
SKL\_ULT/BGA

### CPU1C

SKL\_ULT



SKL\_ULT/BGA



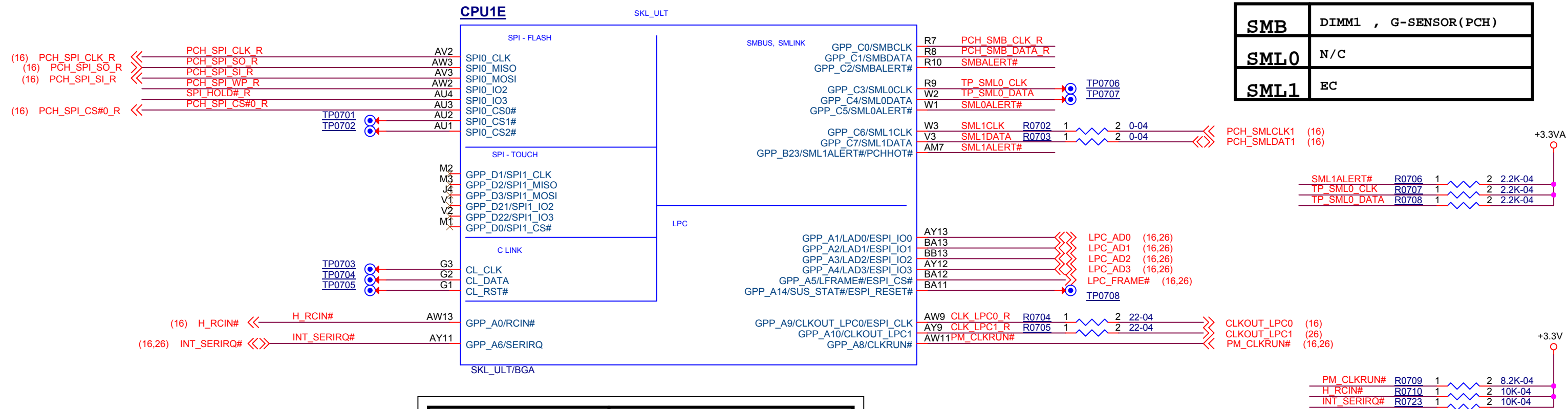
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Title						SKYLAKE-U DDR3L							
Size		Document				Number		NS4SL01				Rev	
Custom												A	
Date:		Friday, October 30, 2015				Sheet		5		of		34	







SMBUS	Device	SMBUS Address
SMB	DDR3 SO-DIMM0	0xA0
	G SENSOR	0x1E
SML0	N/A	N/A
SML1	EC	
	+V CORE PWM	0x20

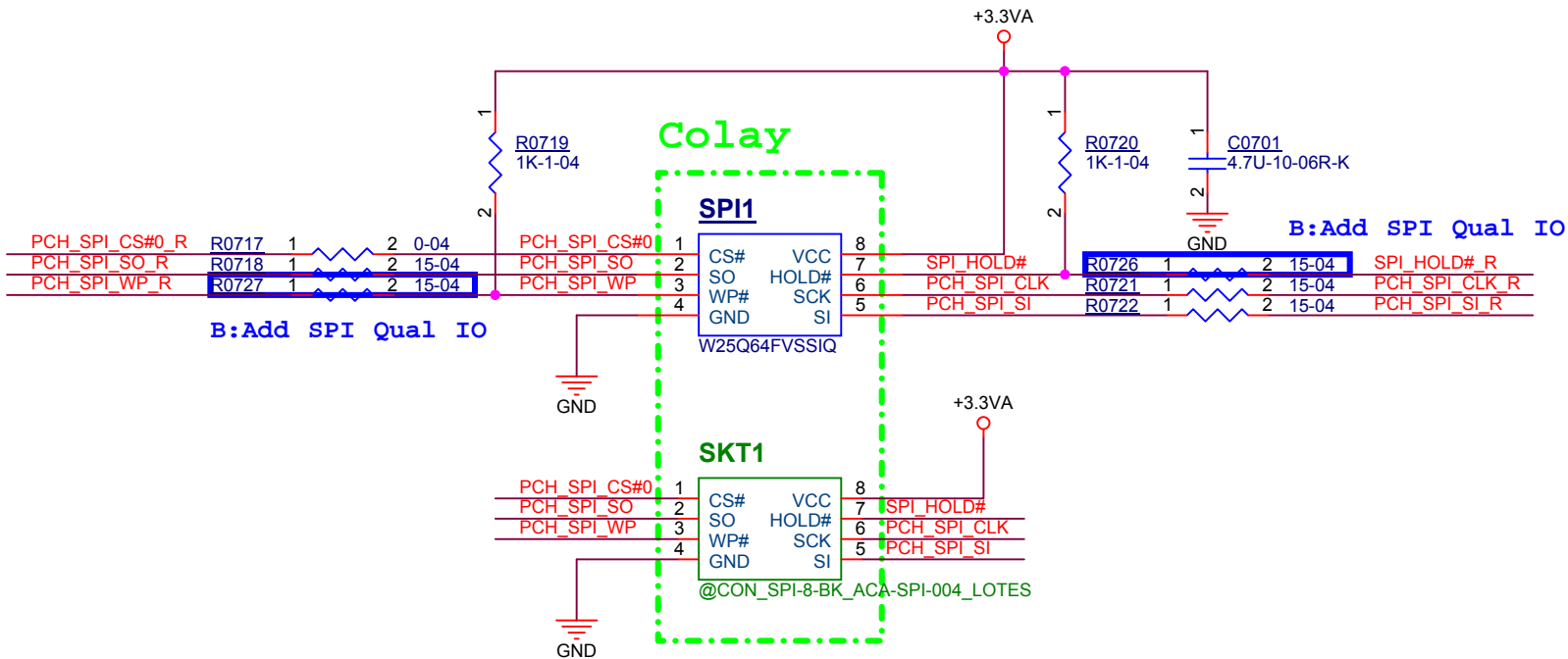
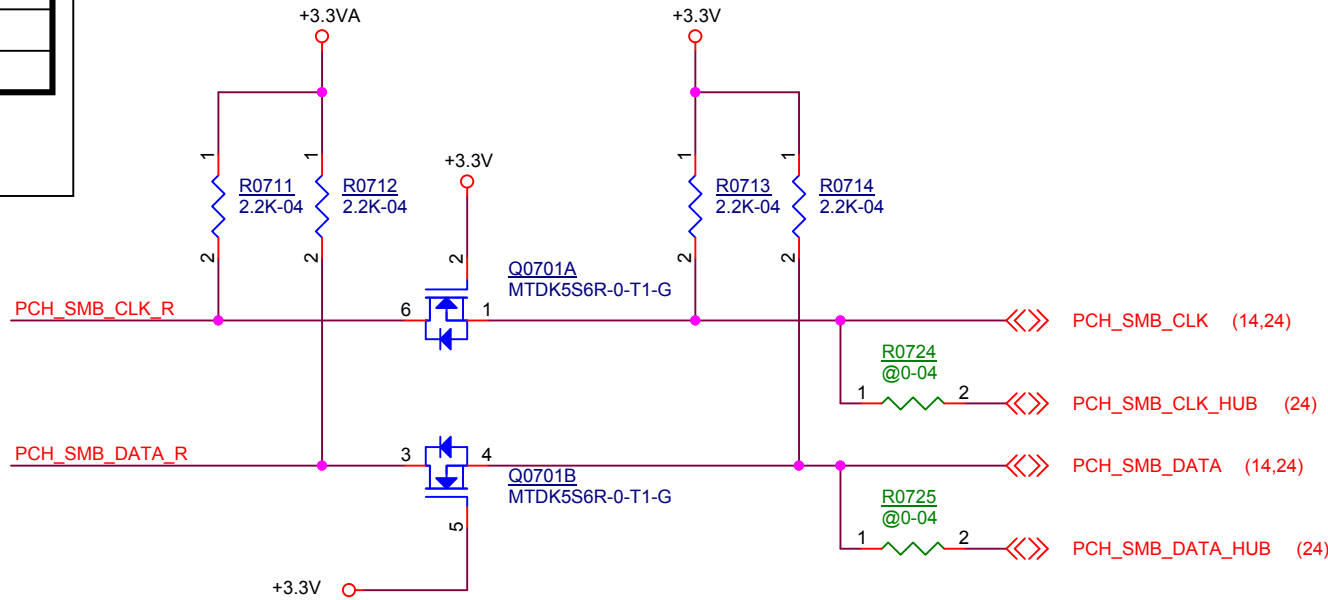
SMBALERT#(IPD)	Intel ME Crypto Transport Layer Security Confidentiality (TLS)
0	Disable (Default)
1	Enable

SMBALERT# R0715 1 2 2.2K-04 +3.3VA

SML0ALERT#(IPD)	eSPI&LPC Select
0	LPC (Default)
1	eSPI

SML0ALERT# R0716 1 2 @2.2K-04 +3.3VA

B: Del\_For LPC



D

D

C

C

B

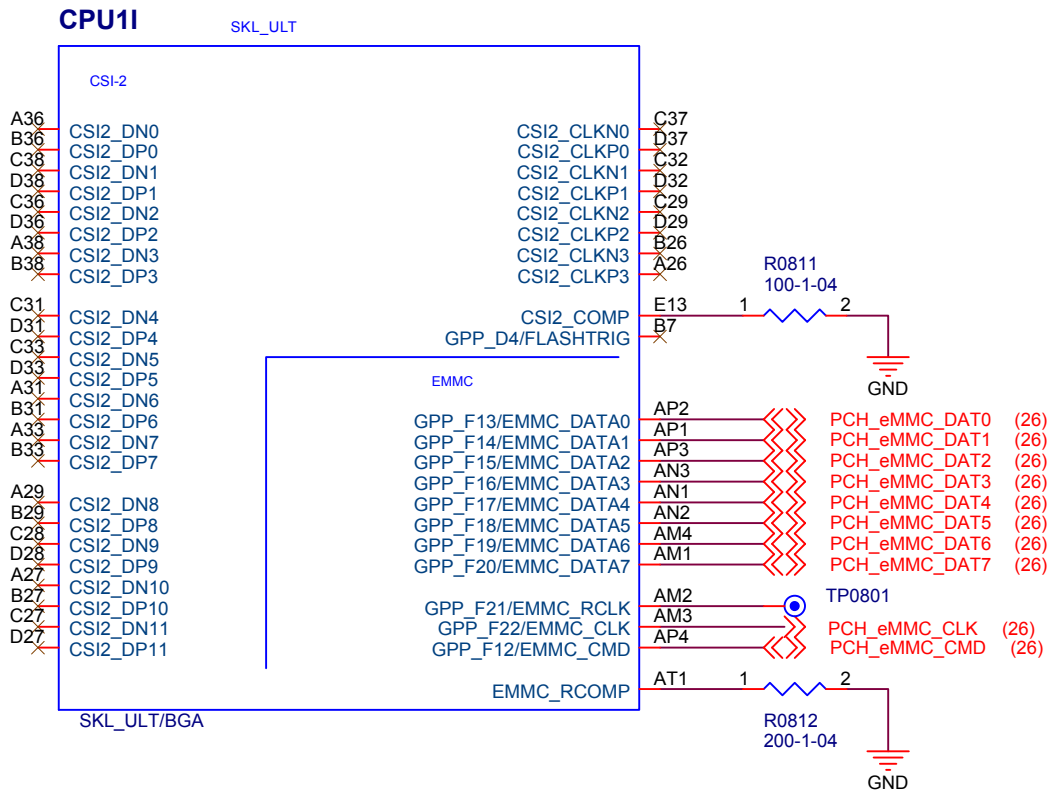
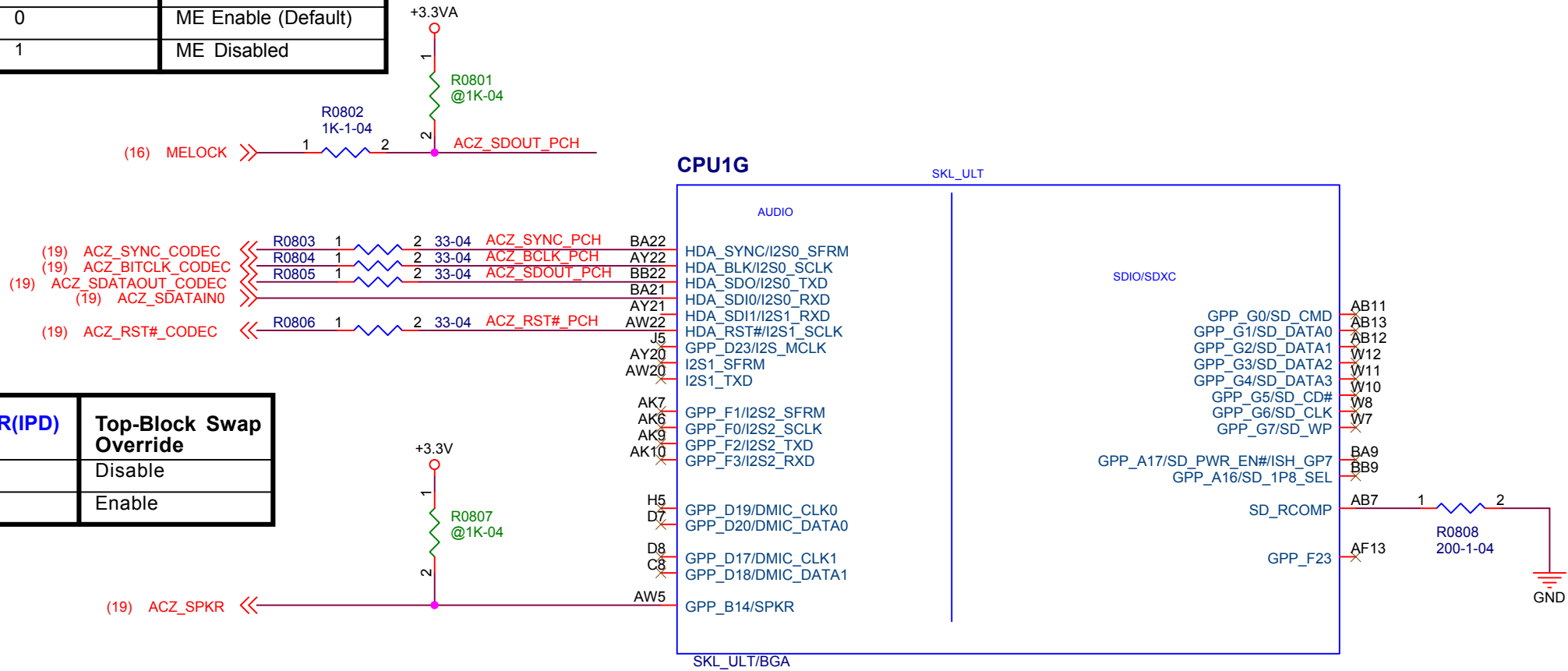
B

A

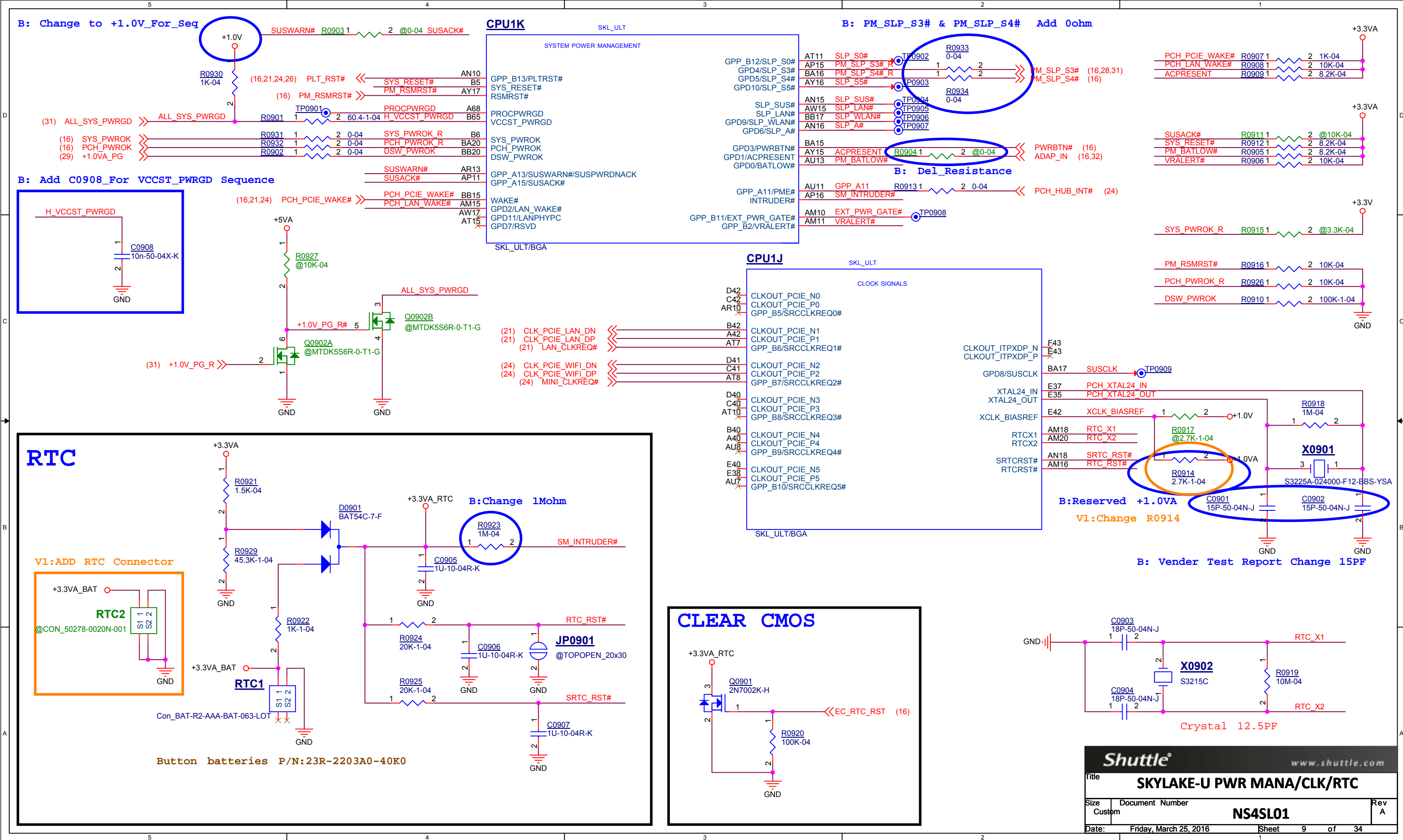
A

ACZ_SDOUT_PCH(IPD)	Flash Descriptor Security Override
0	ME Enable (Default)
1	ME Disabled

ACZ_SPKR(IPD)	Top-Block Swap Override
0	Disable
1	Enable







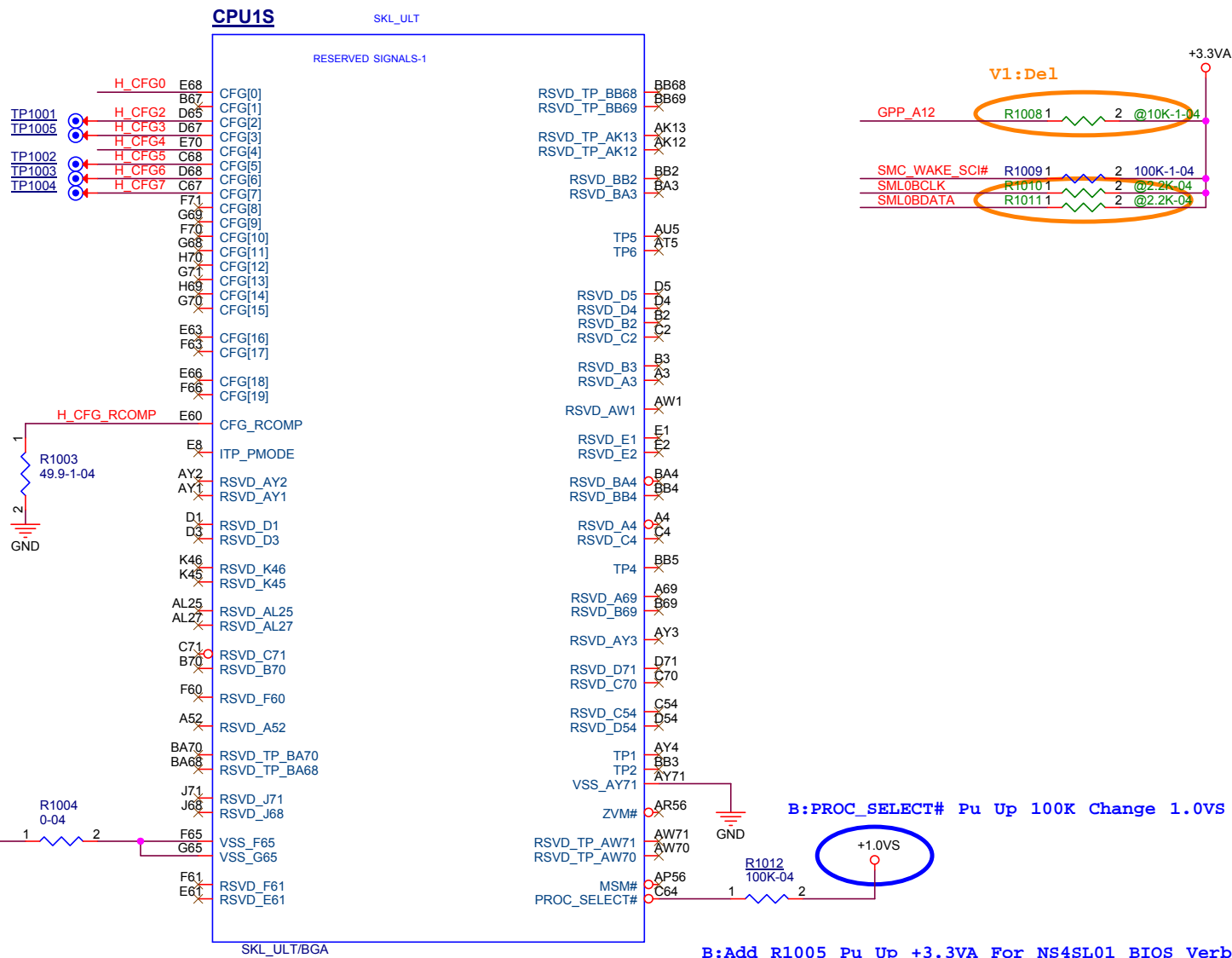
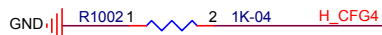
H_CFG0	Stall reset sequence after PCU PLL lock until de-asserted
0	Stall
1	Normal Operation : No stall. (Default)



H_CFG4	eDP Presence strap
0	A Display Port device is connected to the Embedded Display Port.
1	No Physical Display Port attached to Embedded DisplayPort*

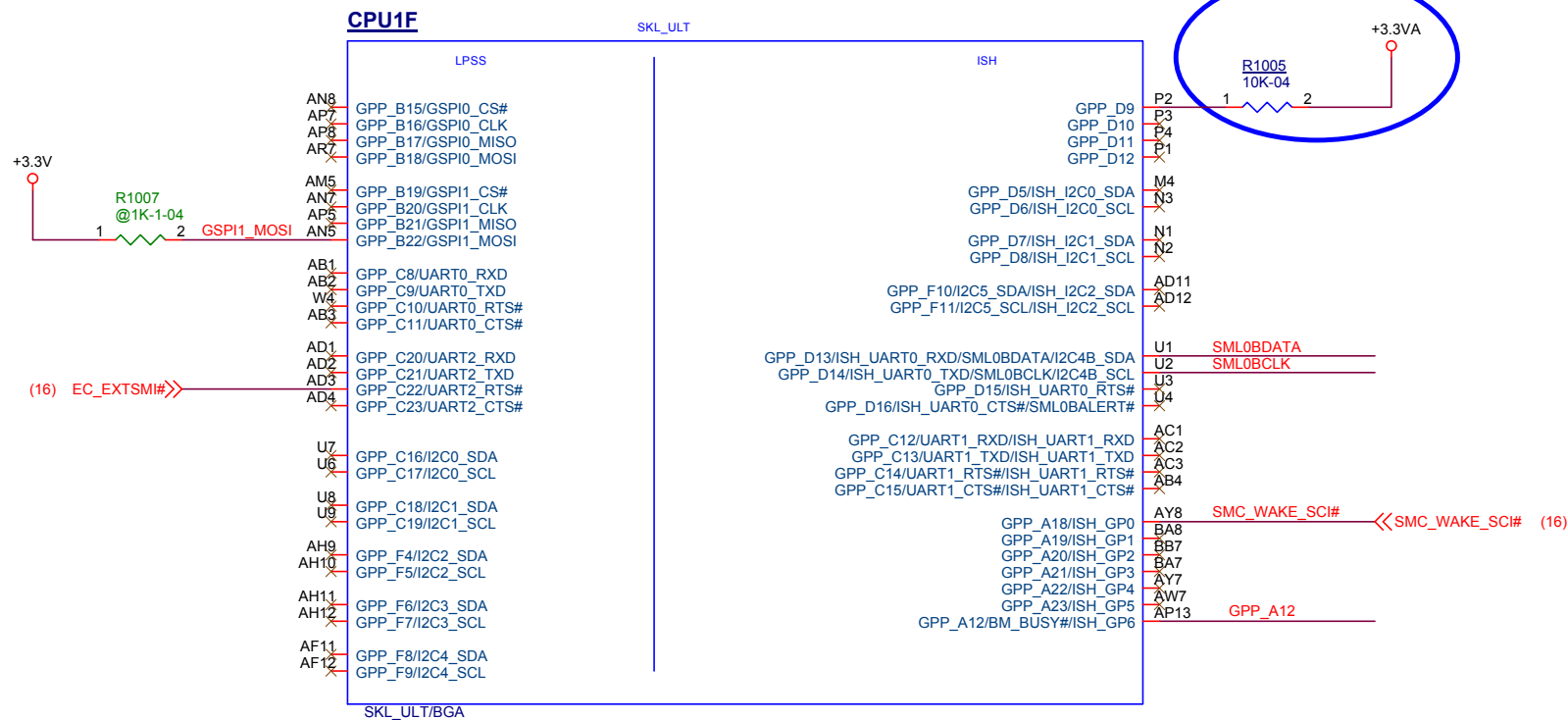
  

GND. ||| R1002 1 2 1K-04 H\_CFG4

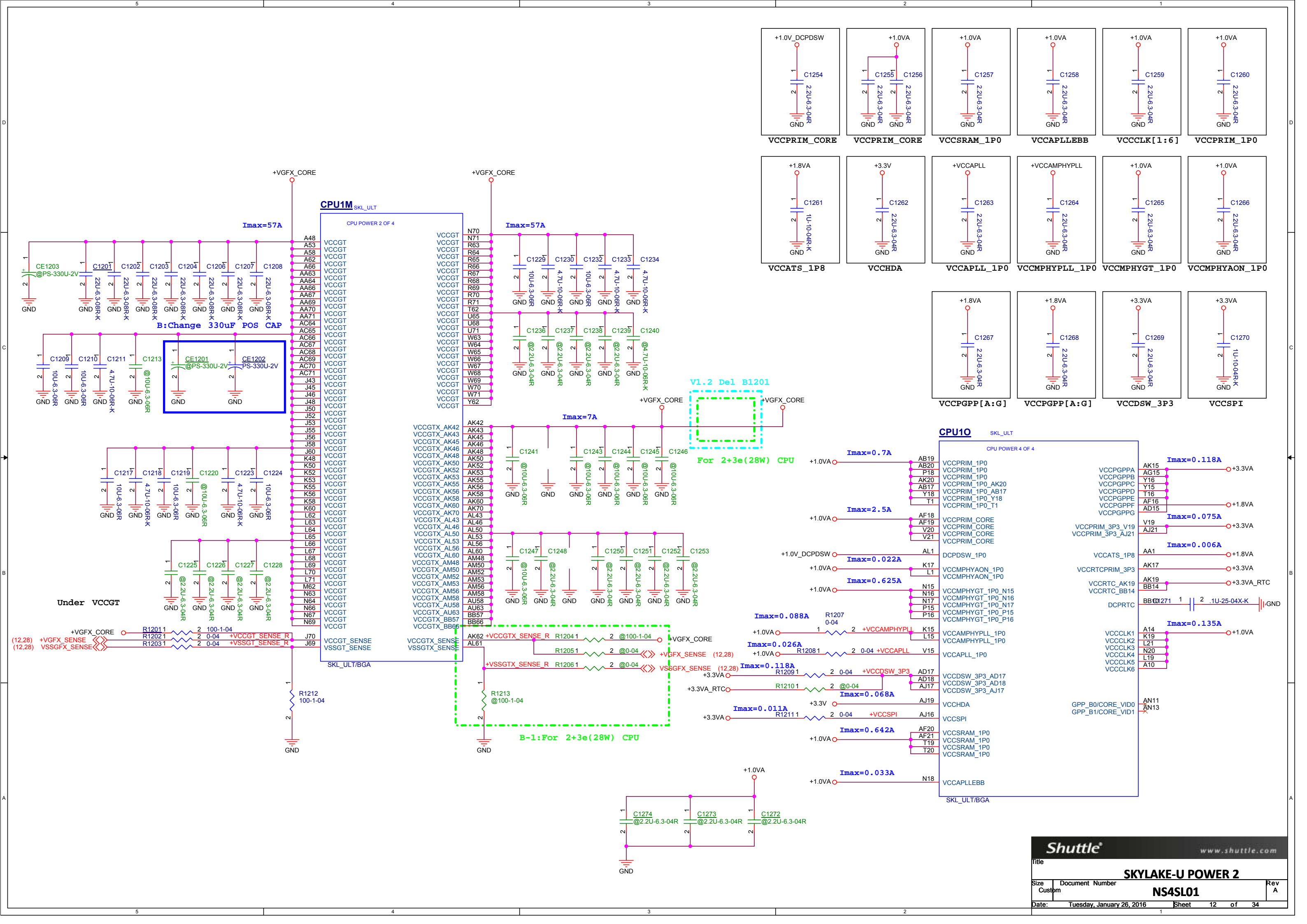


GSPI0_MOSI(IPD)	No Reboot Mode with TCO Disabled
0	Disabled (Default)
1	Enable

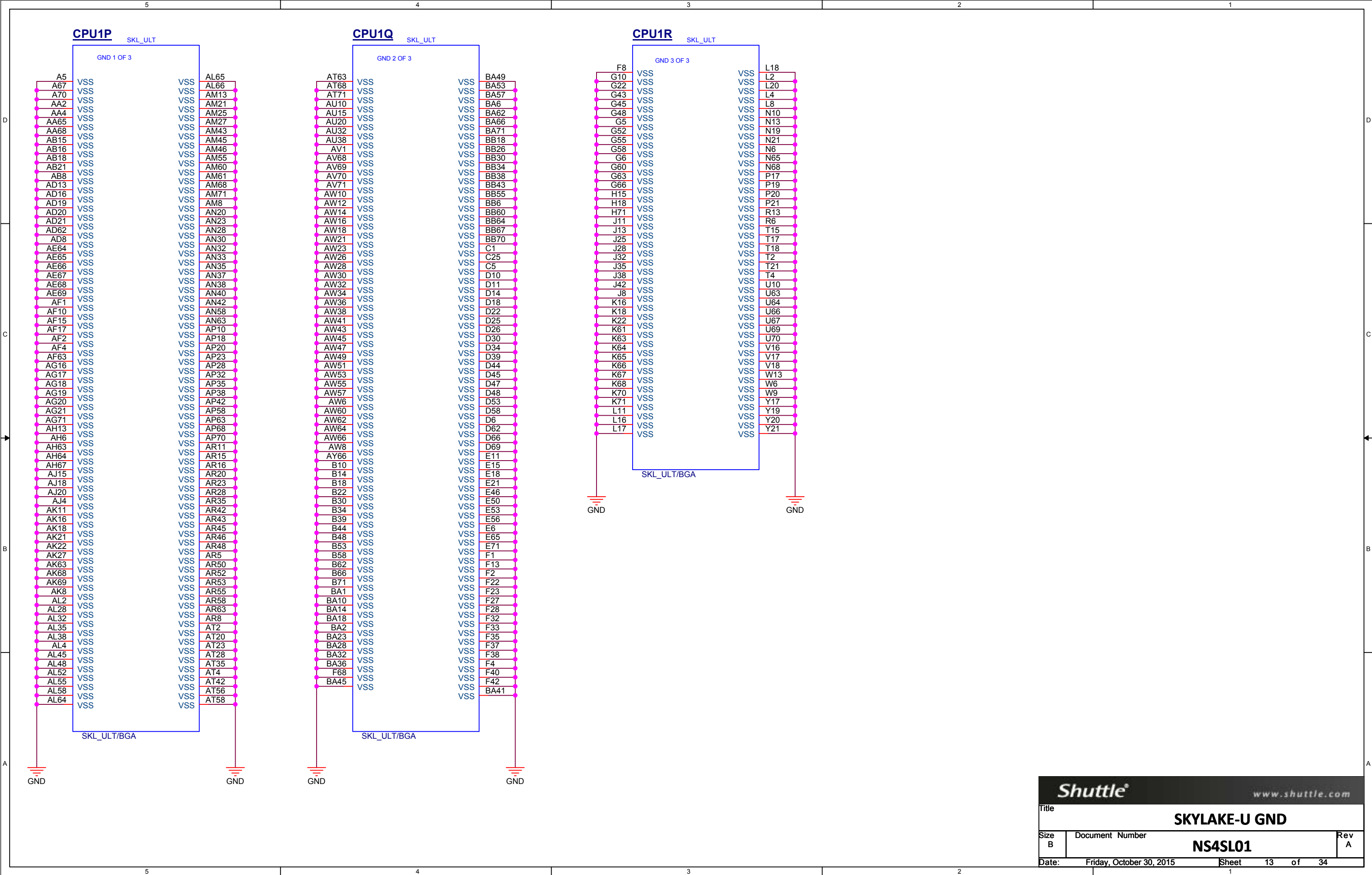
<b>GSPi1_MOSI(IPD)</b>	<b>Boot BIOS Destination</b>
0	SPI (Default)
1	LPC



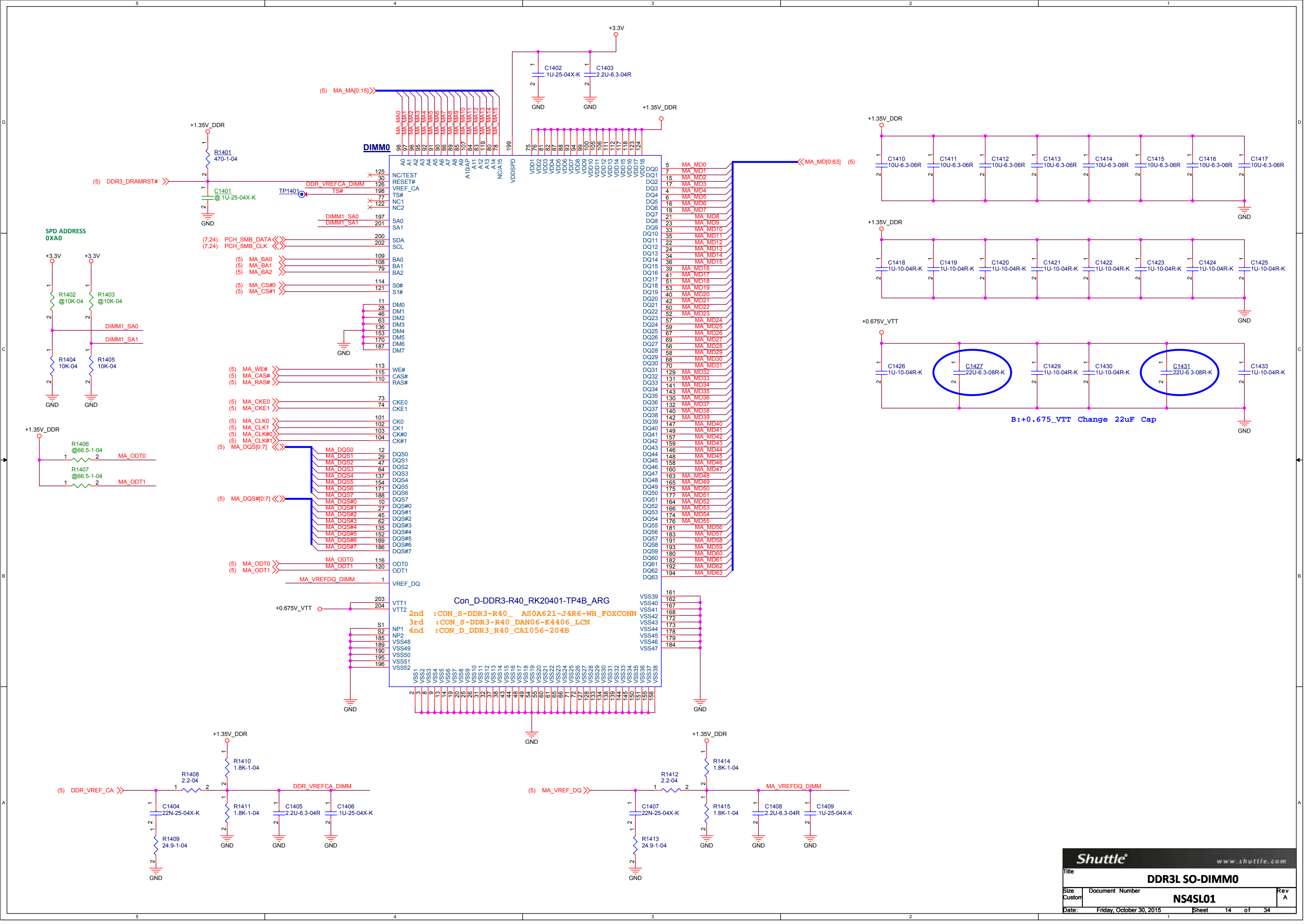






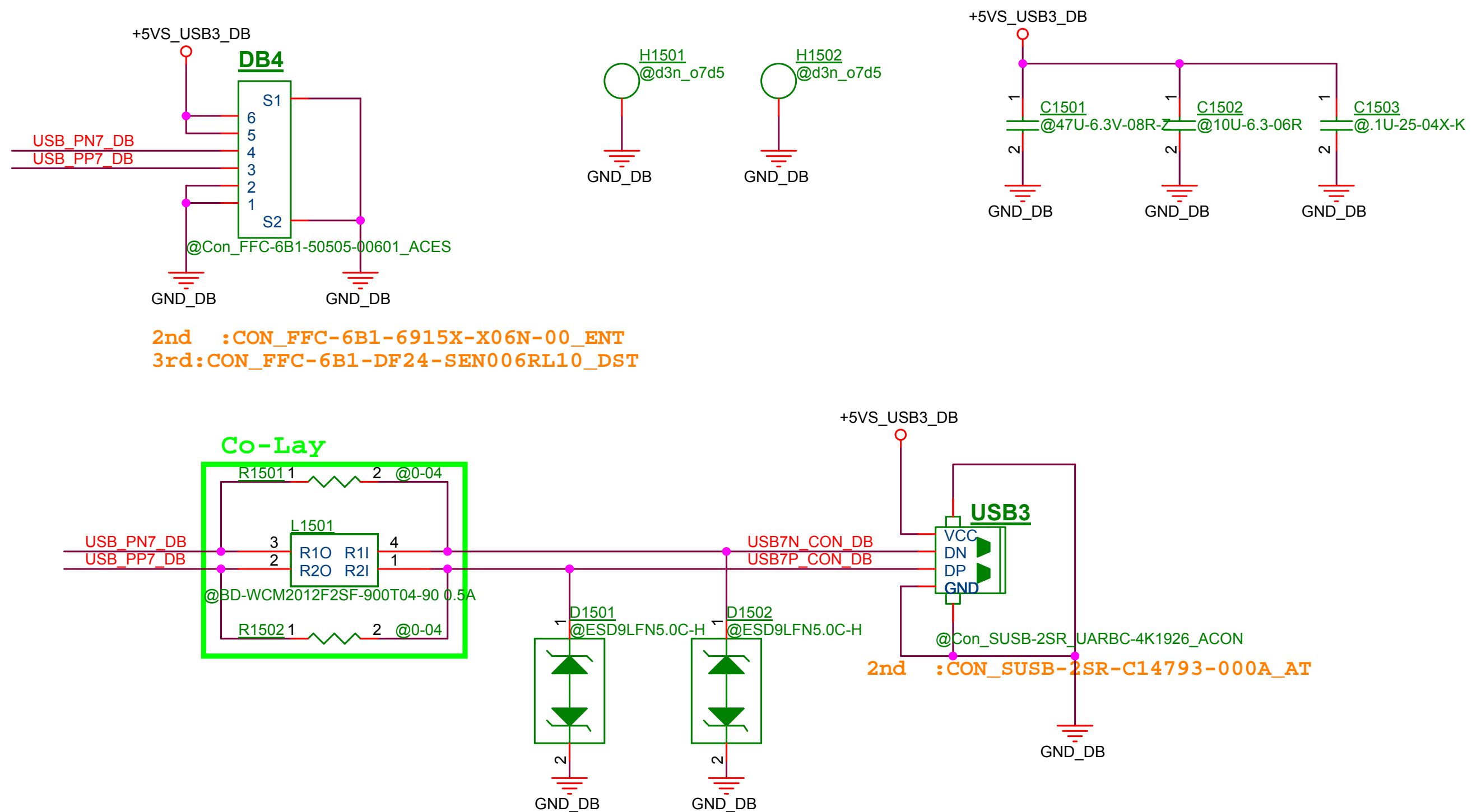






# USB2.0\_IO\_DB

## B: Add USB2.0 D/B



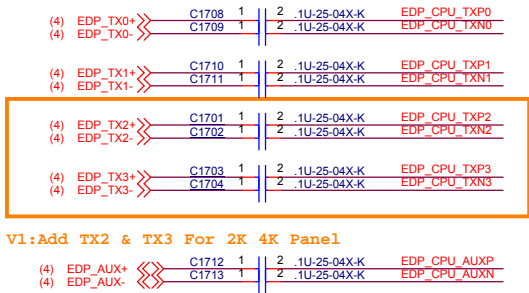
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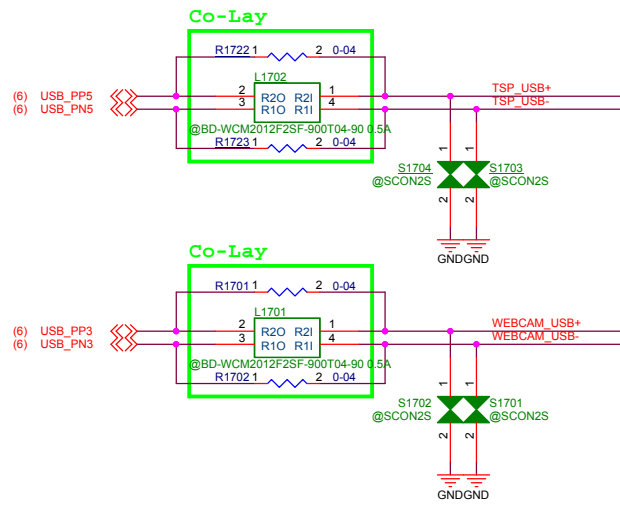
Title			USB2.0_D/B_BD		
Size	Document Number				Rev
A	NS4SL01				A
Date:	Thursday, November 05, 2015		Sheet	15 of 34	



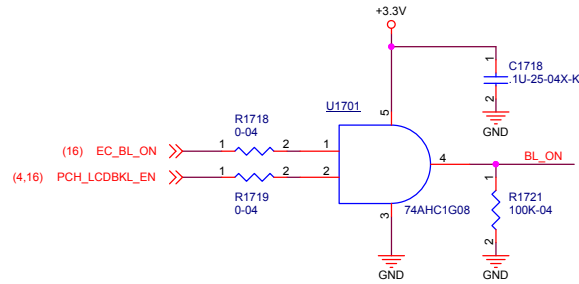
## eDP\_Interface



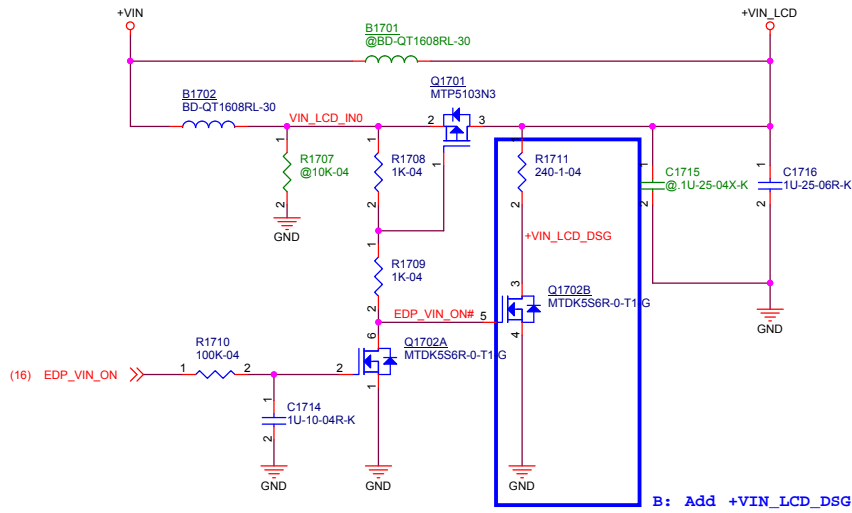
## USB\_Interface



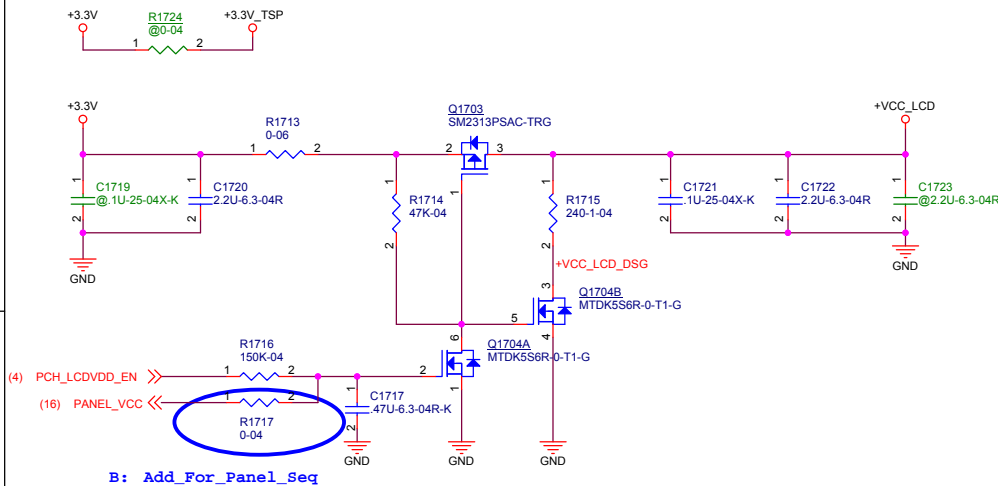
## BL\_Enable



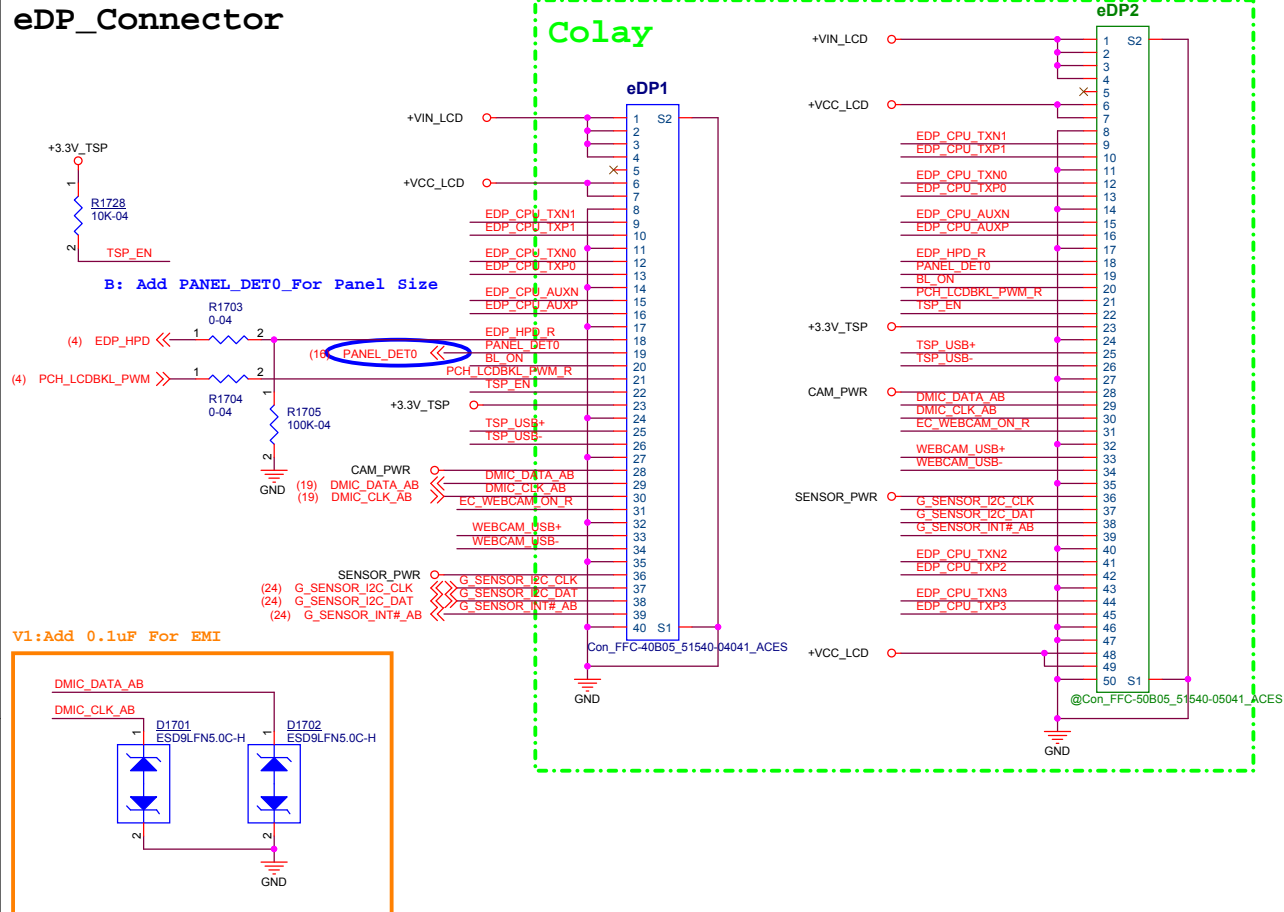
## BL\_PWR



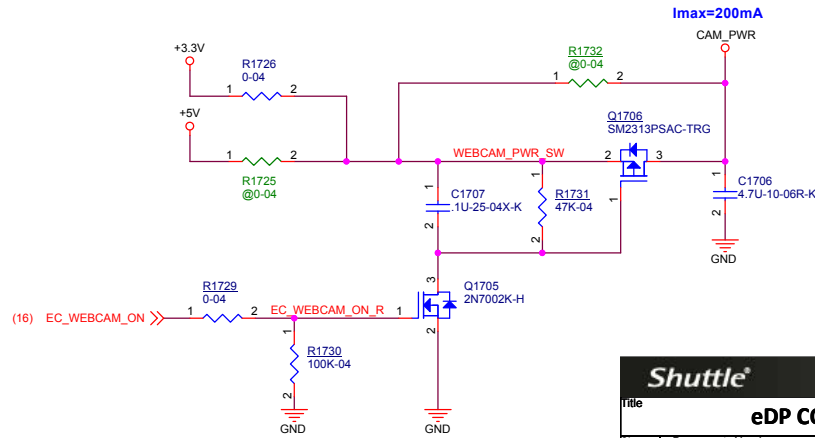
## Panel\_PWR & TSP\_PWR

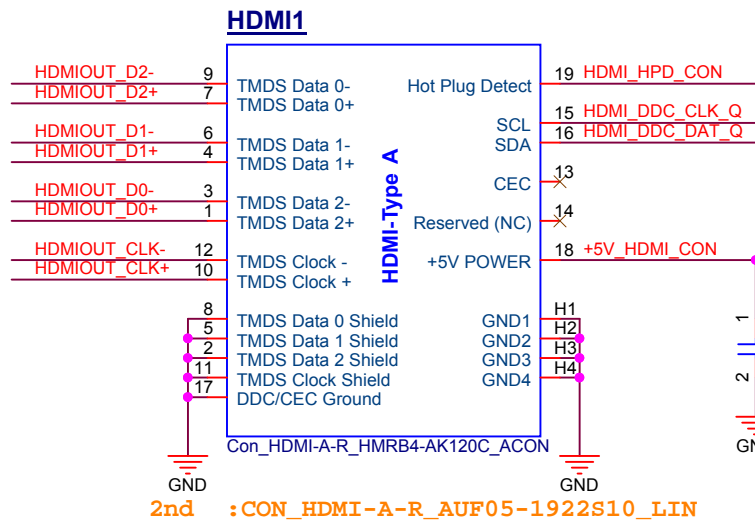
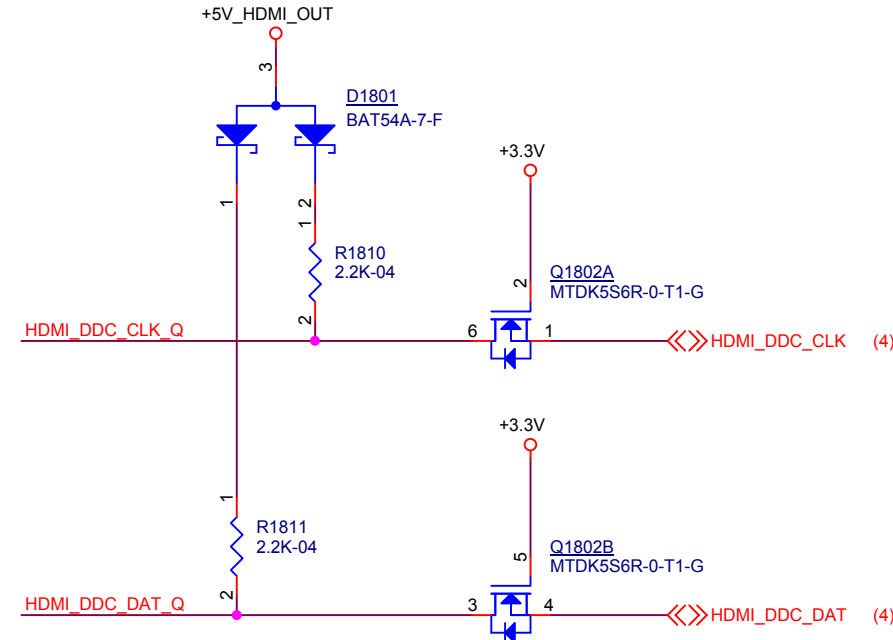
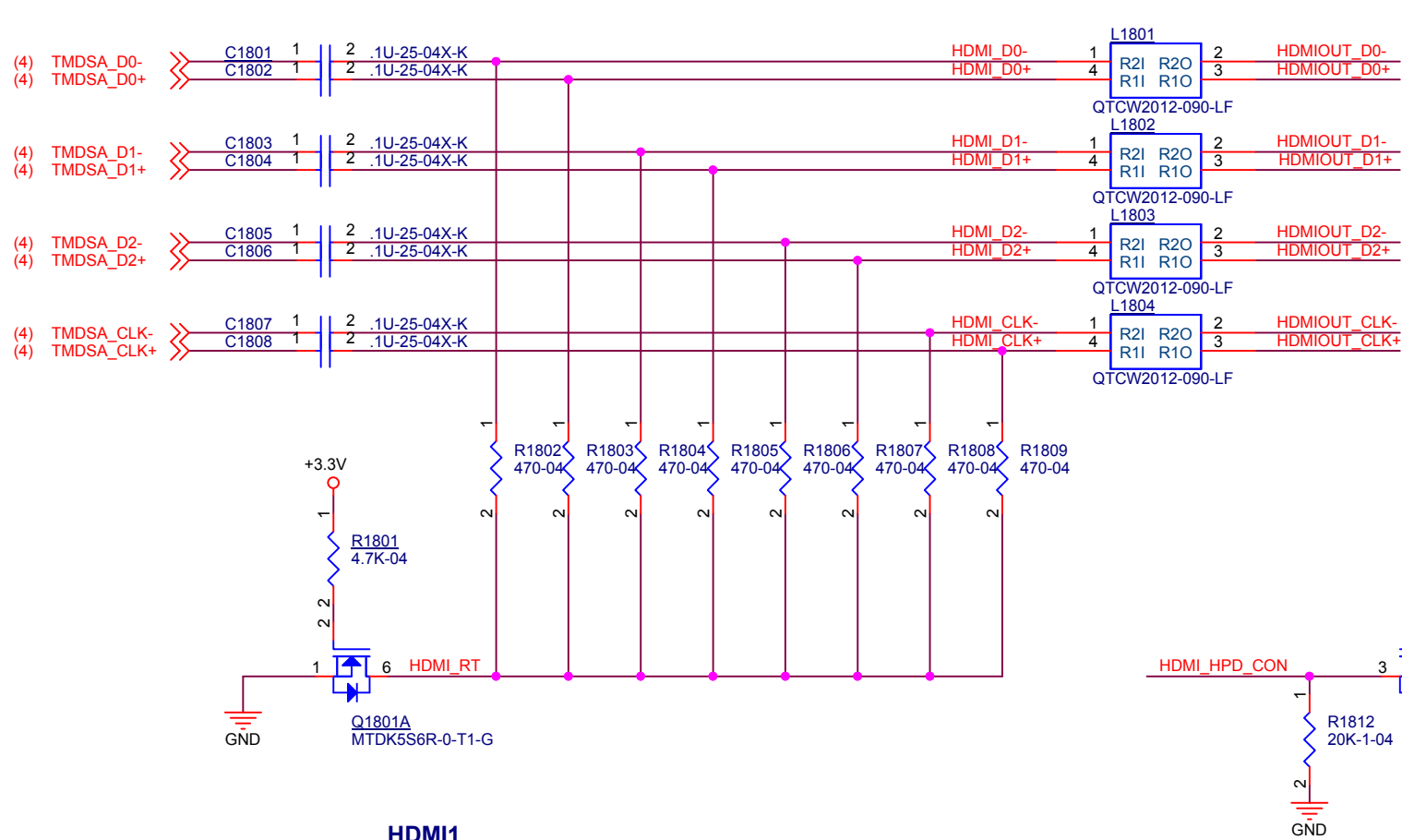


## eDP\_Connector



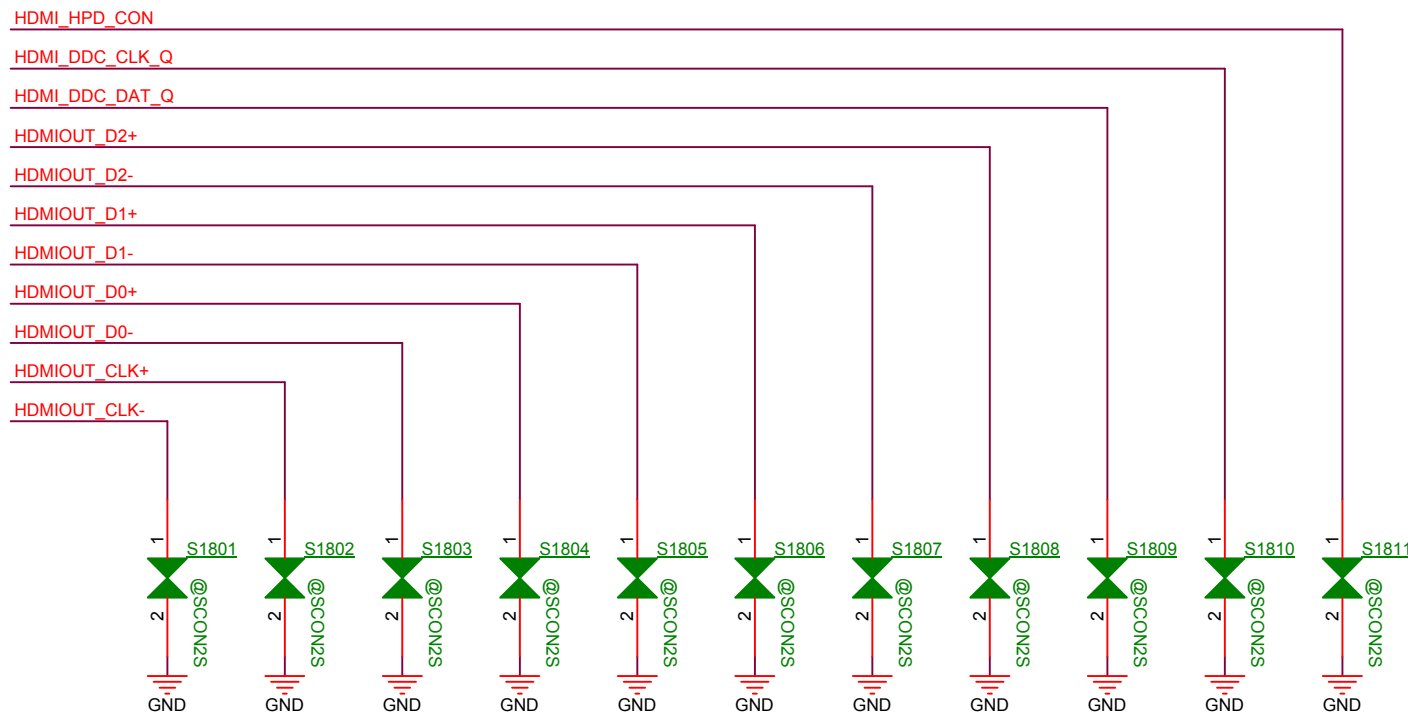
## Camrea\_PWR





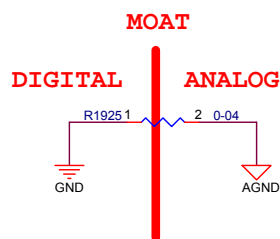
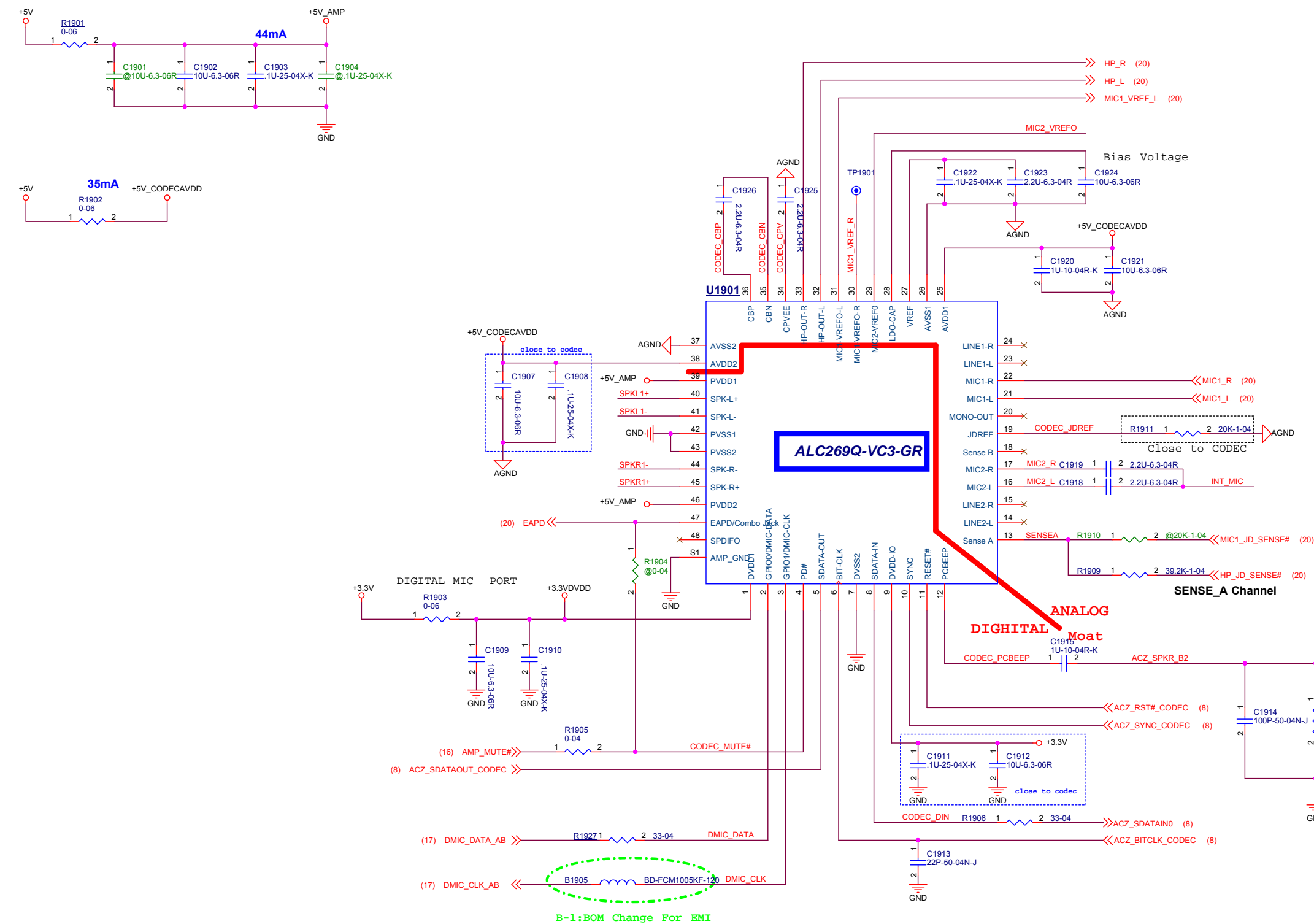
2nd :CON\_HDMI-A-R\_AUF05-1922S10\_LIN

Port 2	DDI2_TXP[0]	DDI2_LANE0_DP	HDMIx_TX2_DP
	DDI2_TXN[0]	DDI2_LANE0_DN	HDMIx_TX2_DN
	DDI2_TXP[1]	DDI2_LANE1_DP	HDMIx_TX1_DP
	DDI2_TXN[1]	DDI2_LANE1_DN	HDMIx_TX1_DN
	DDI2_TXP[2]	DDI2_LANE2_DP	HDMIx_TX0_DP
	DDI2_TXN[2]	DDI2_LANE2_DN	HDMIx_TX0_DN
	DDI2_TXP[3]	DDI2_LANE3_DP	HDMIx_CLK_DP
	DDI2_TXN[3]	DDI2_LANE3_DN	HDMIx_CLK_DN
Hot plug detect used by HDMI Port 2		DDPC_HPD	DDI2_HPD_Q
HDMI DDC lines for Port 2		DDPC_CTRLCLK	DDI2_CTRL_CK
		DDPC_CTRLDATA	DDI2_CTRL_DATA

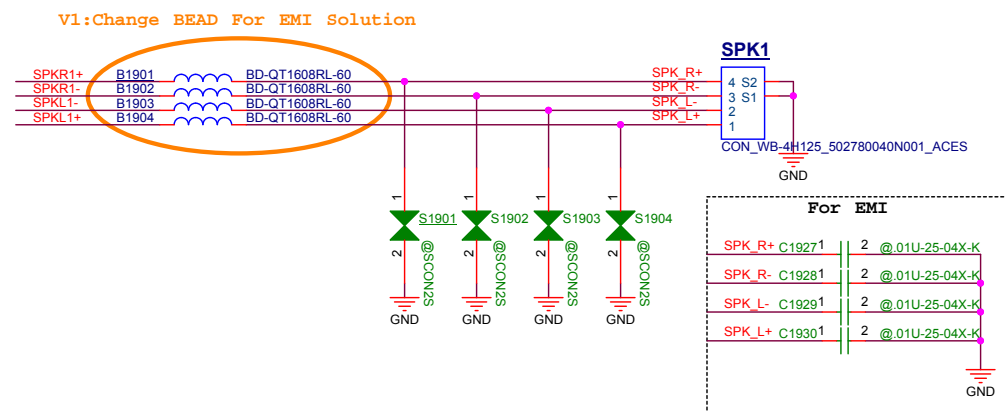




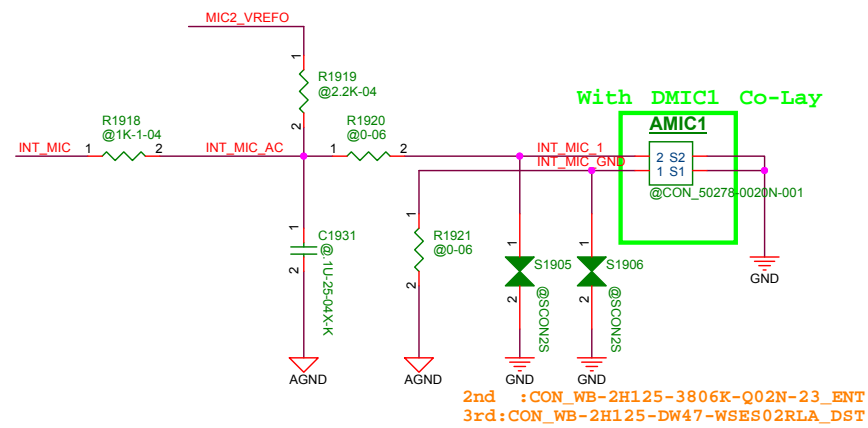
# CODEC ALC269Q



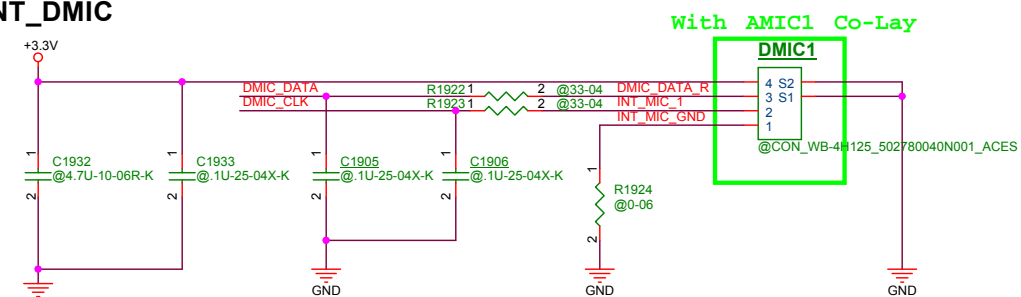
**INT\_SPEAKER**



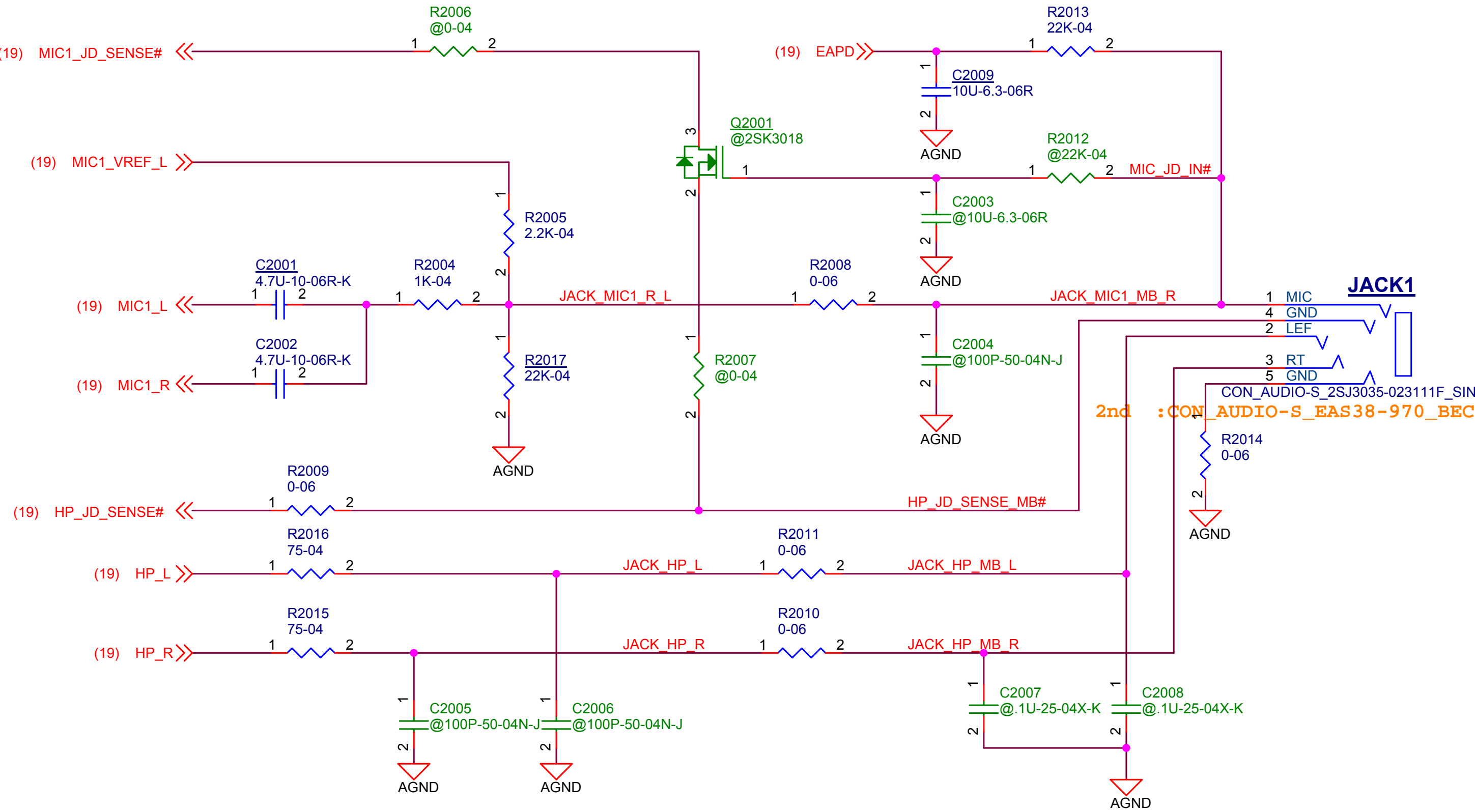
**INT\_AMIC**





## INT\_DMIC



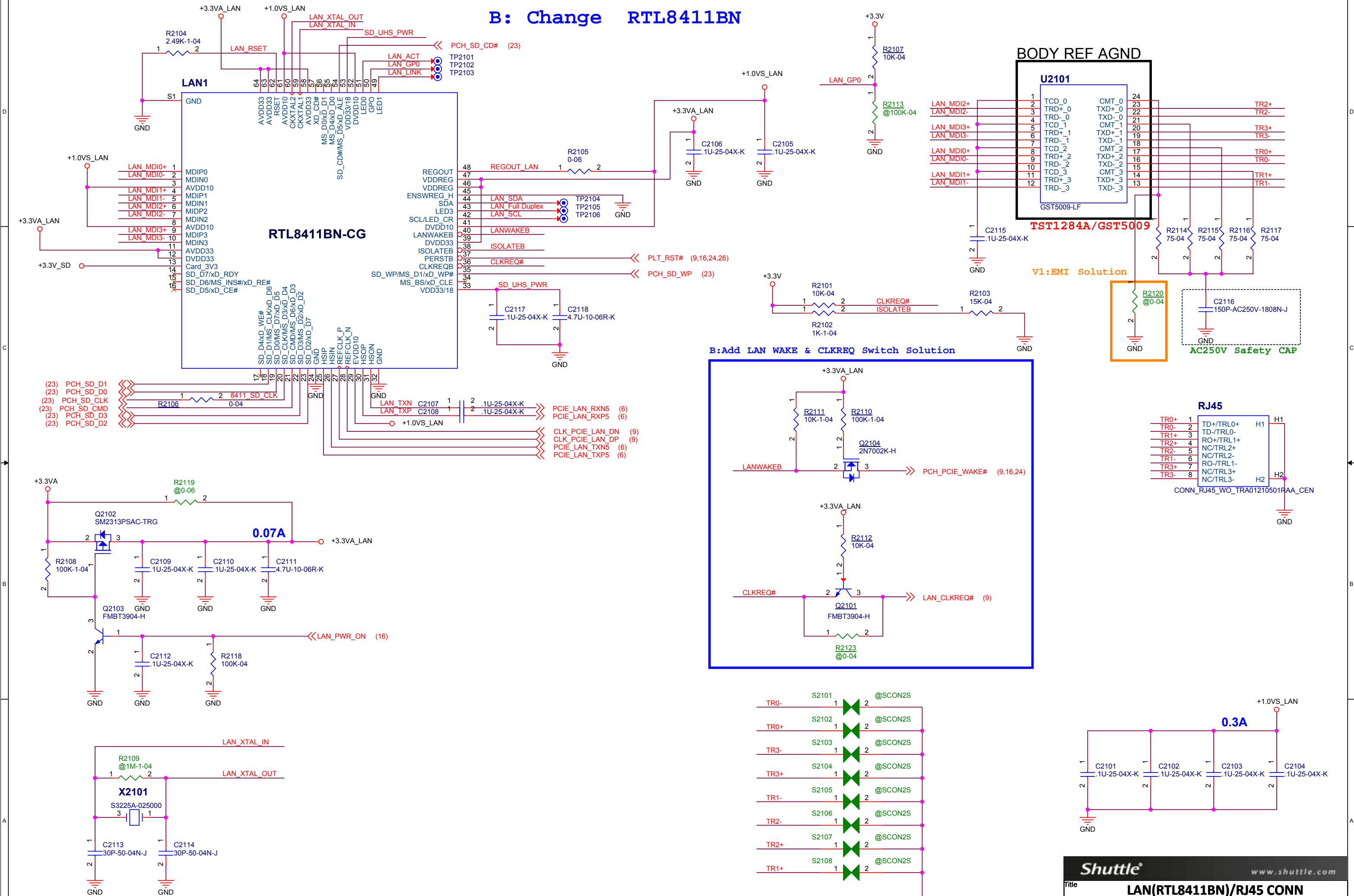
# 2 IN 1 Audio Jack



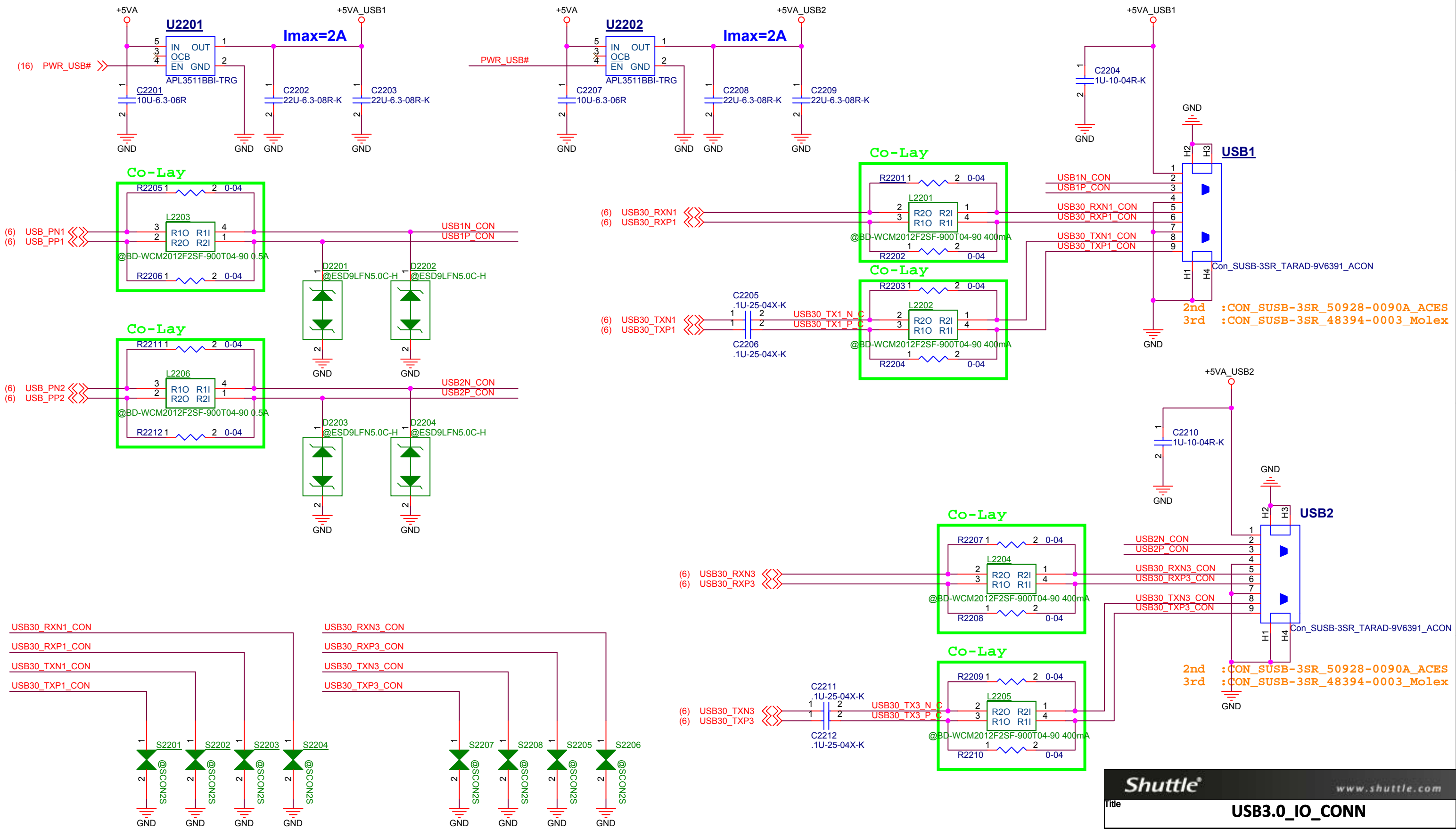


Title			AUDIO JACK		
Size	Document Number				Rev
A	NS4SL01				A
Date:	Friday, October 30, 2015		Sheet	20 of 34	

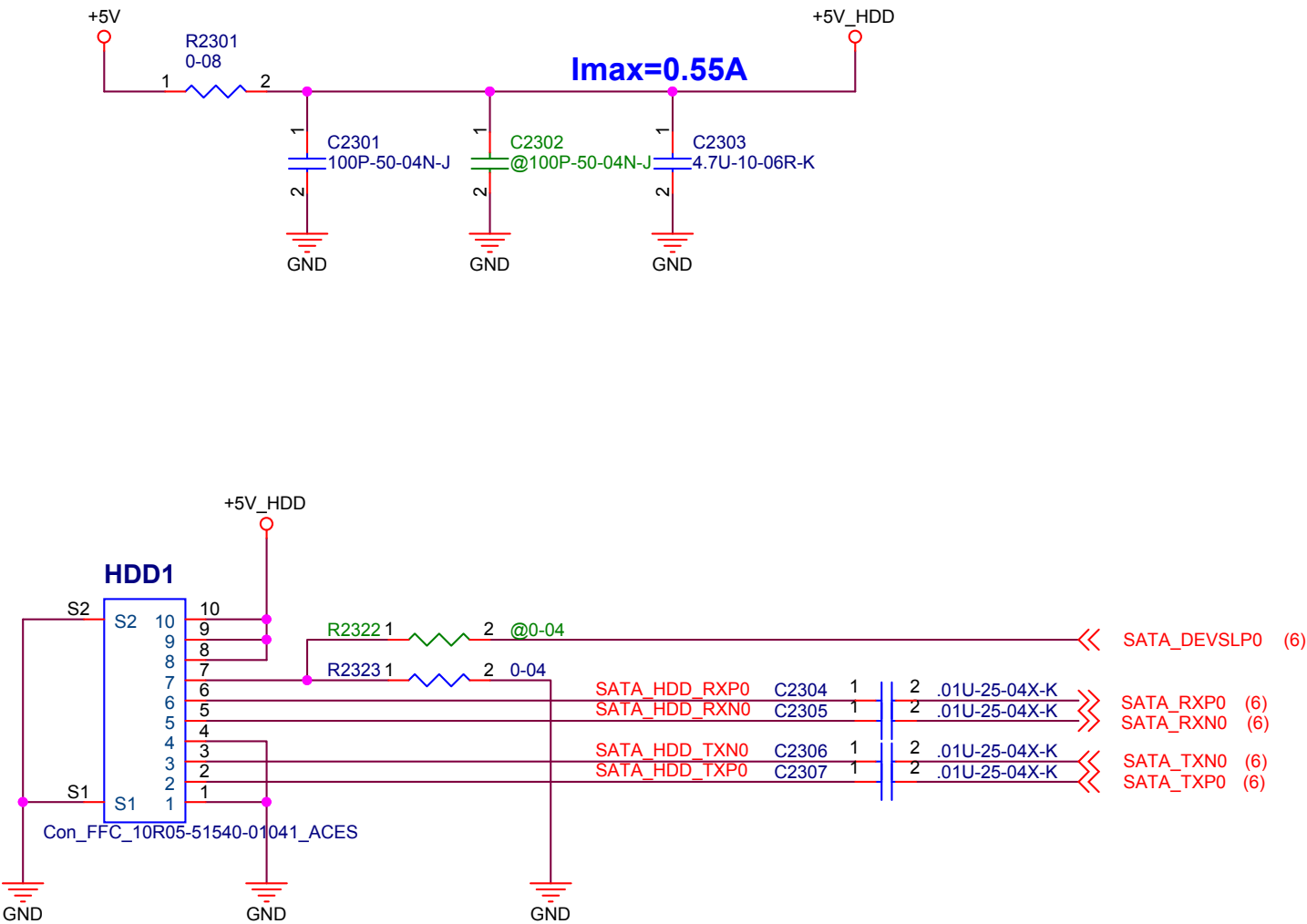
**B: Change**     **RTL8411BN**



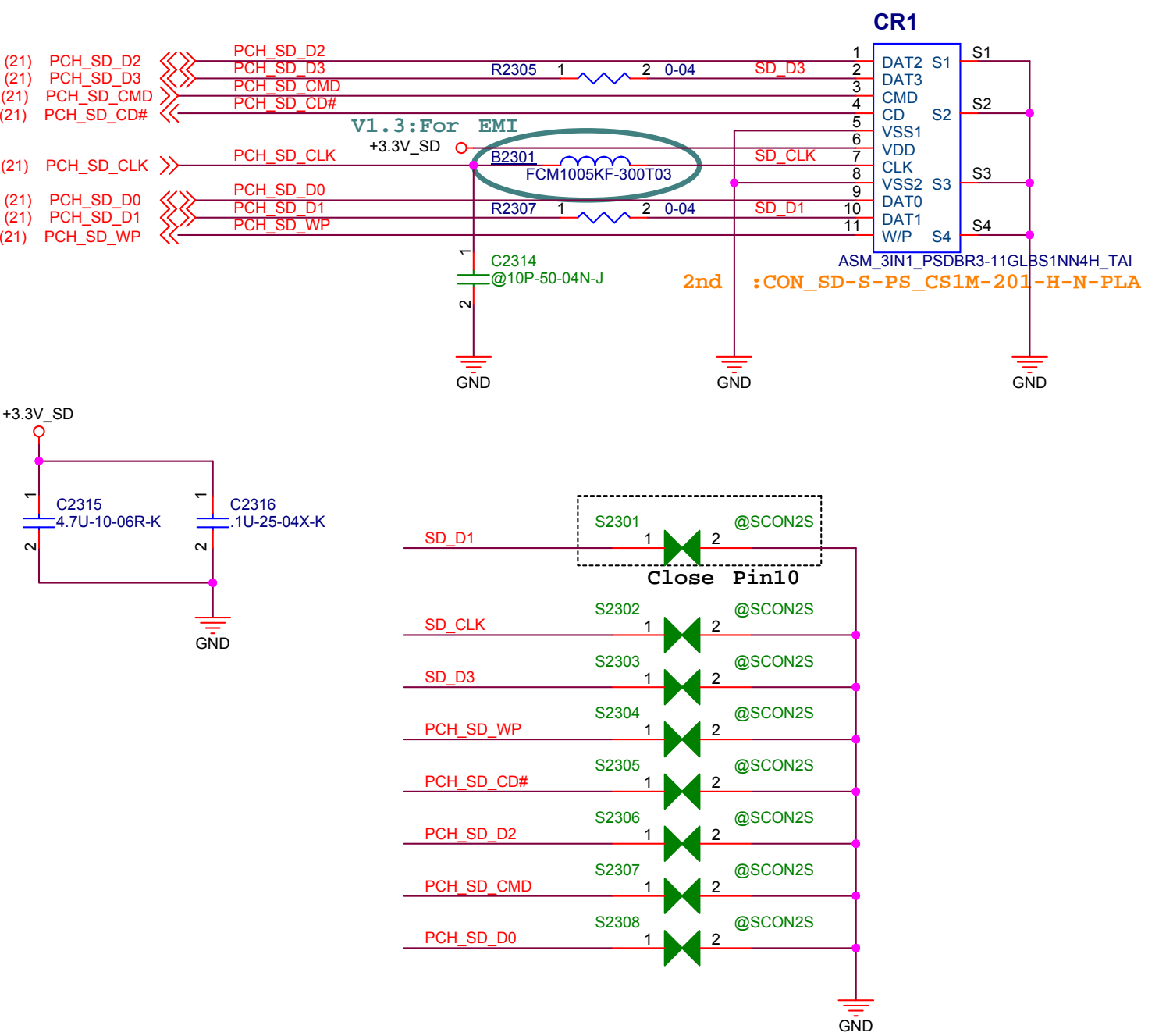
# USB3.0



HDD

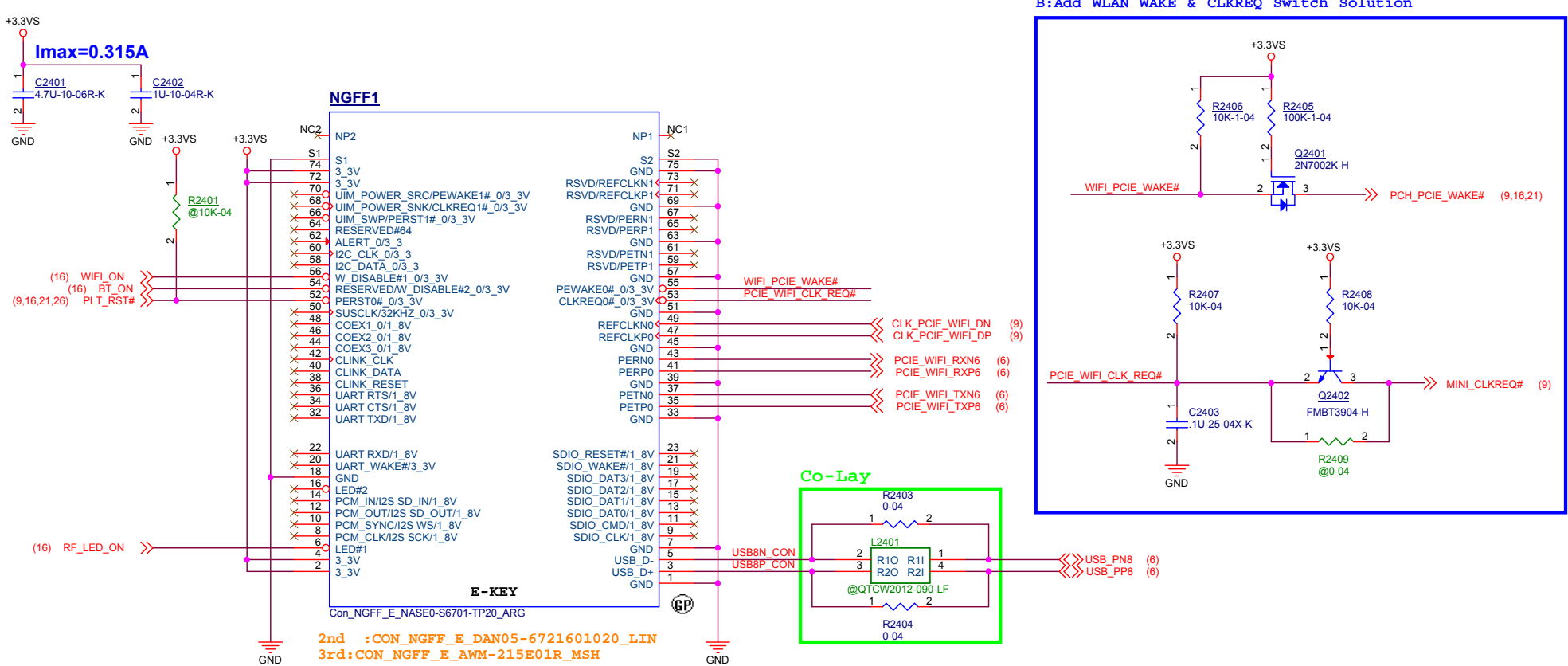


SD CARD CONN

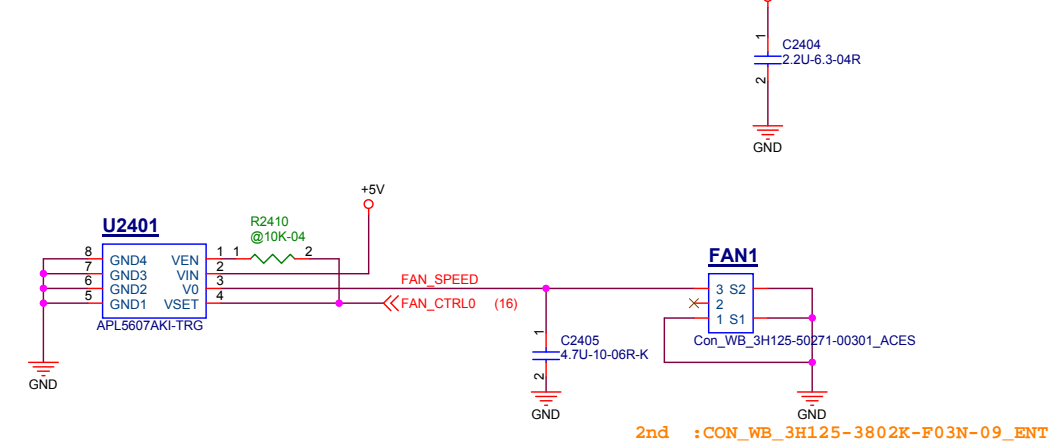




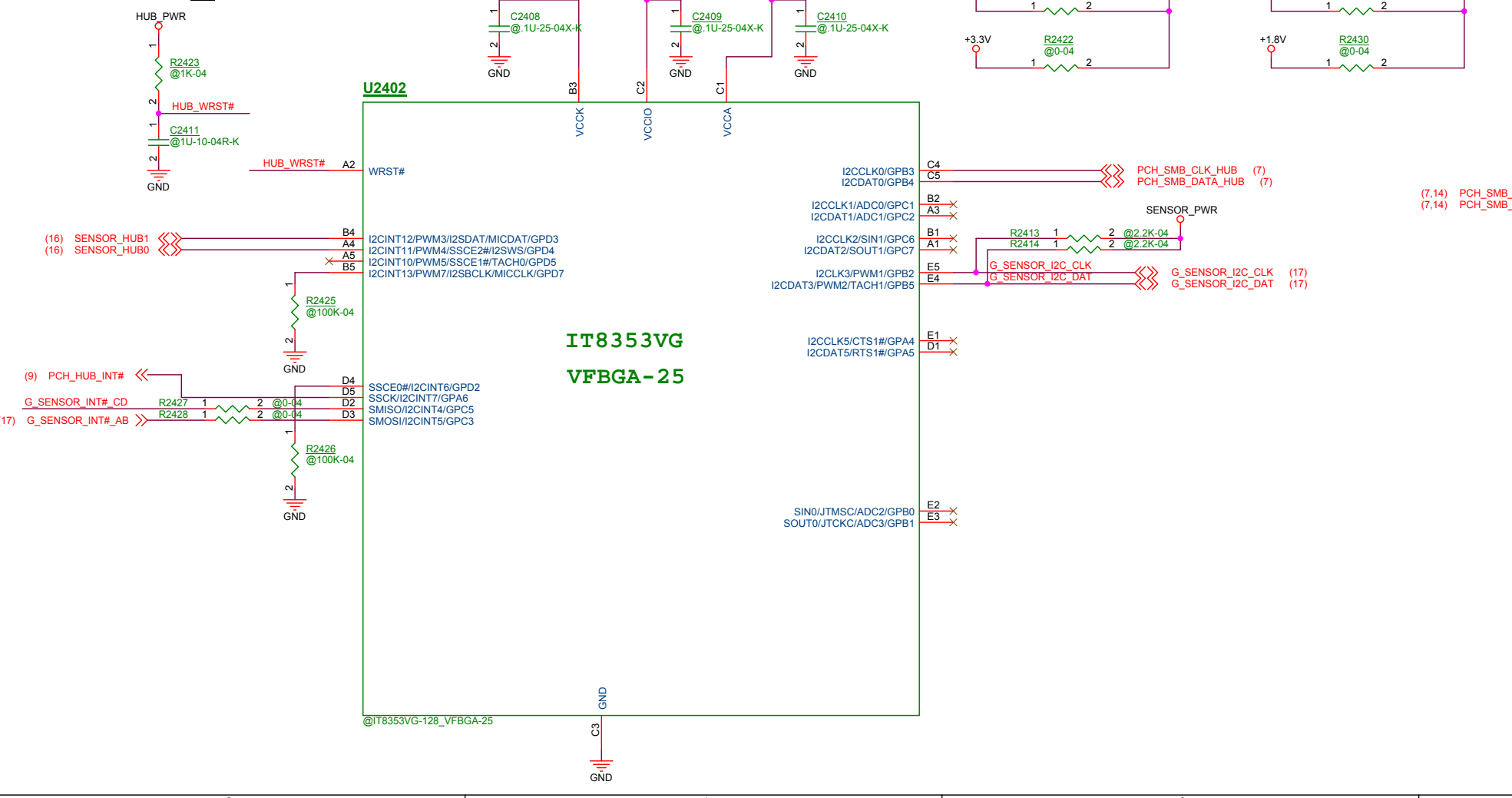
NGFF CONN



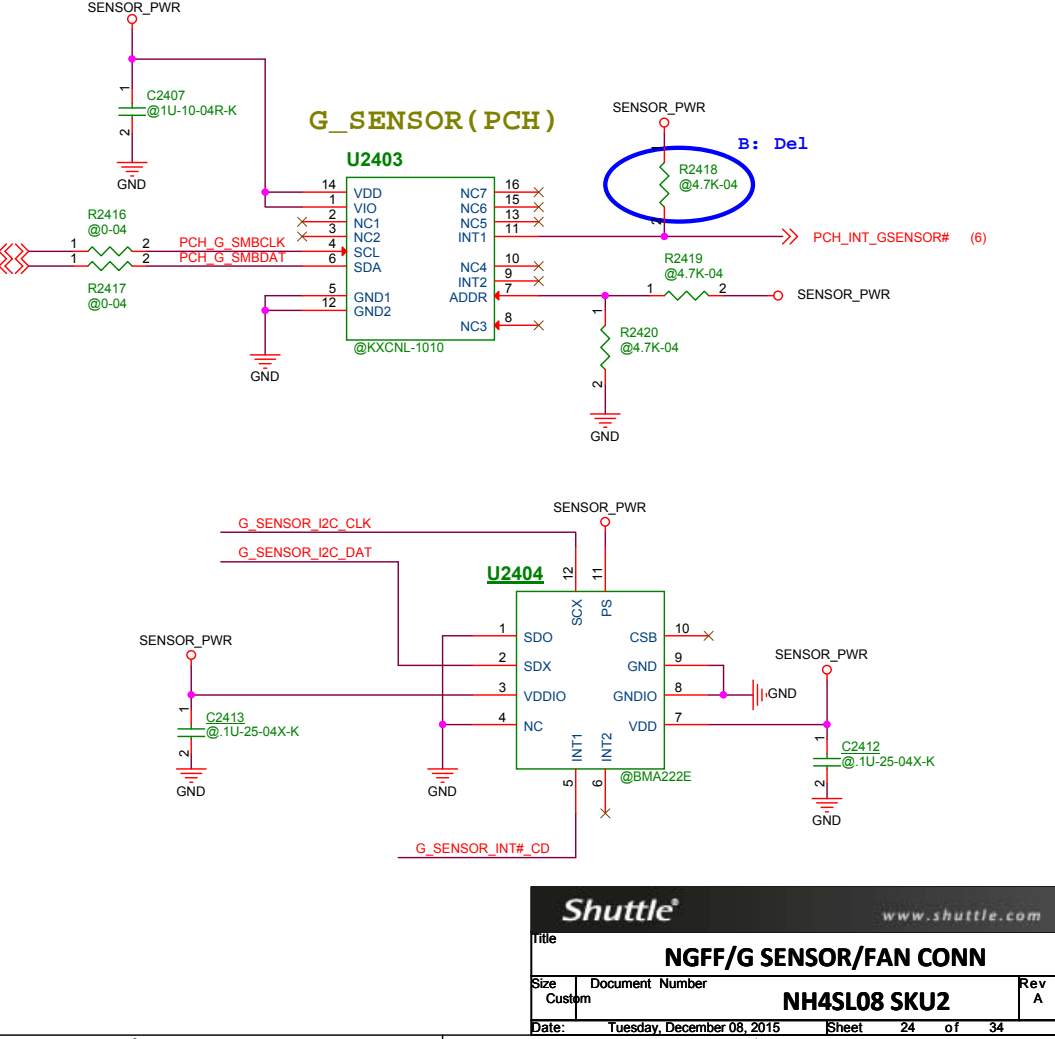
FAN CONTROLLER



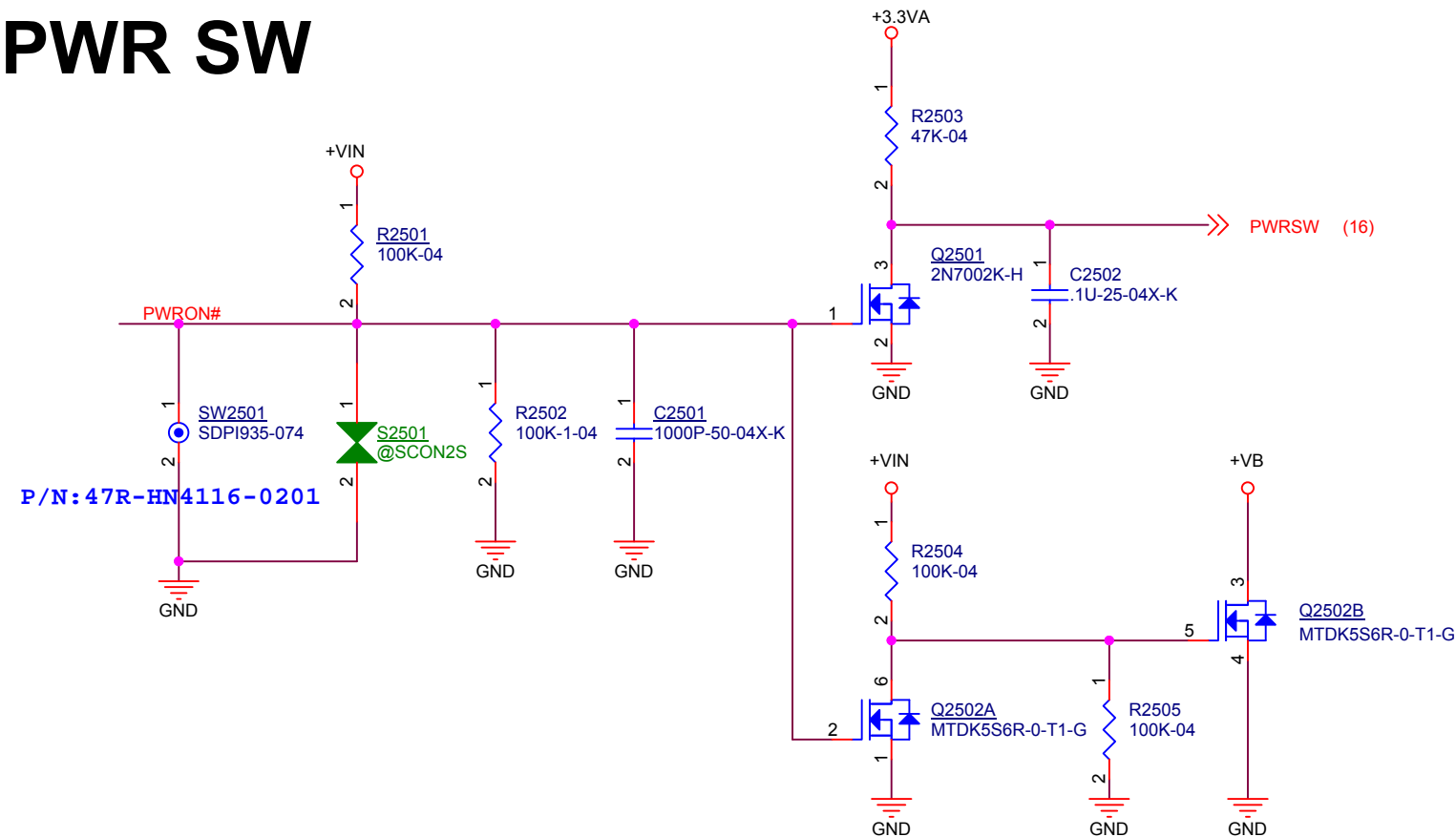
SENSOR\_HUB



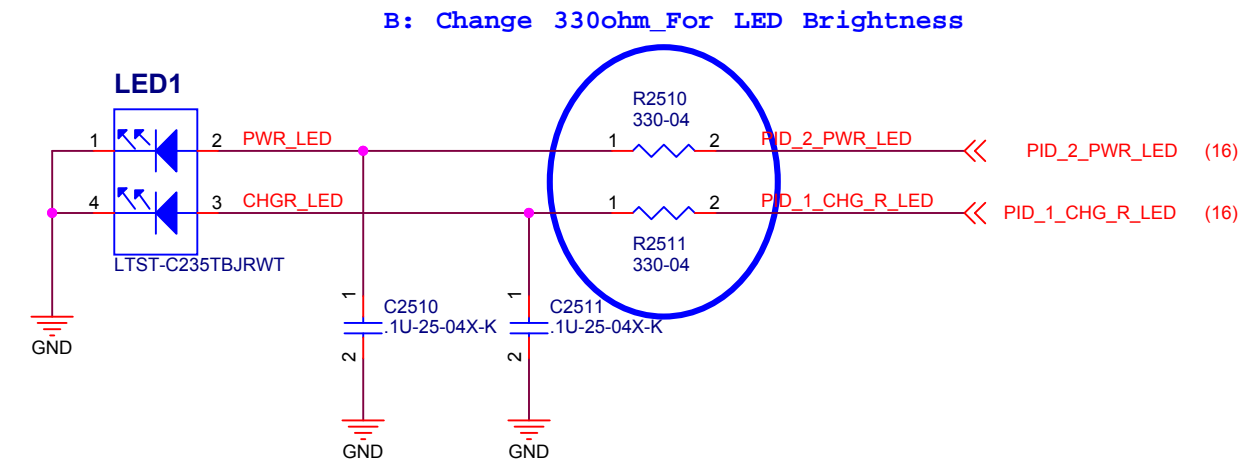
G-SENSOR



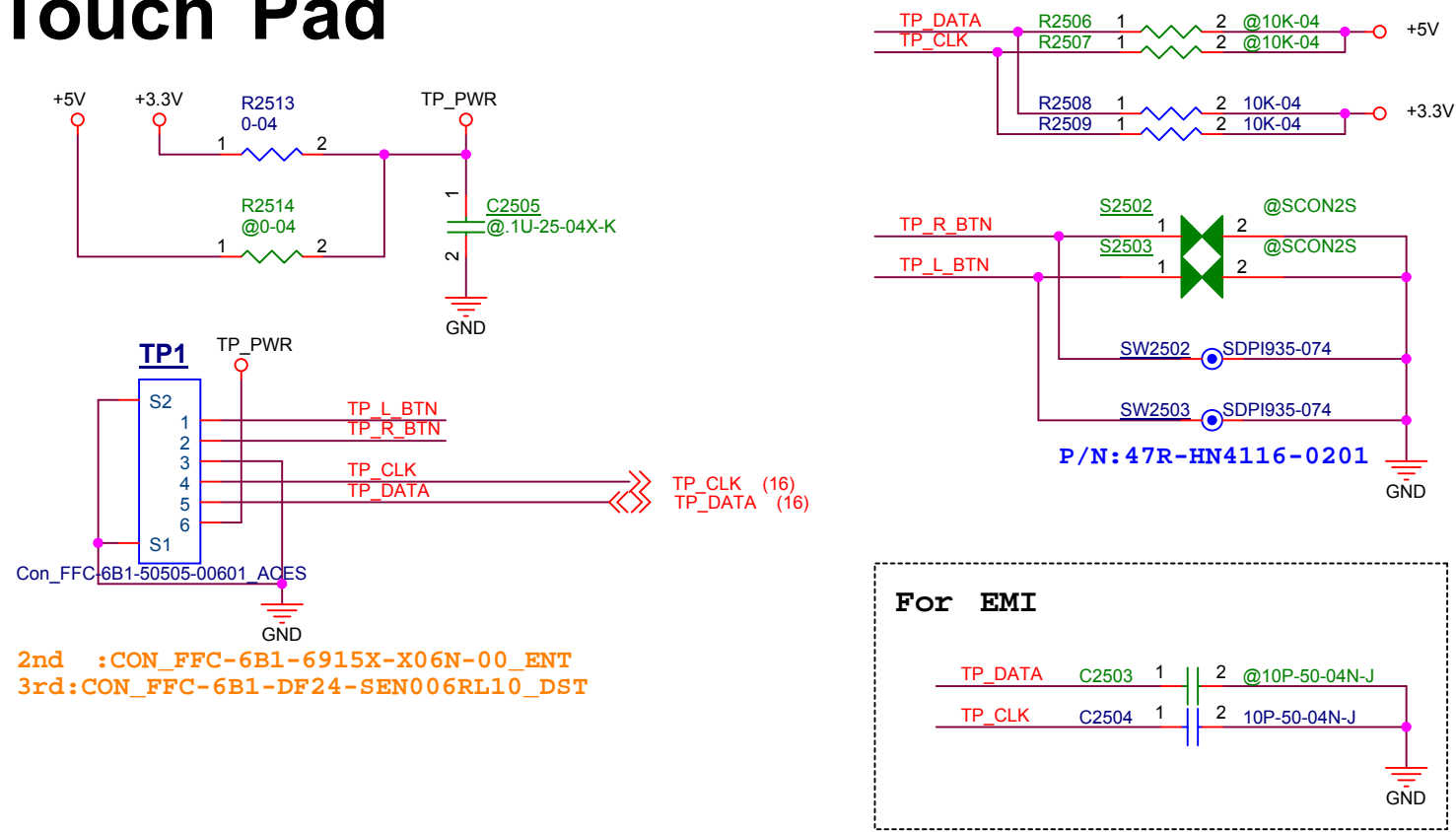
# PWR SW



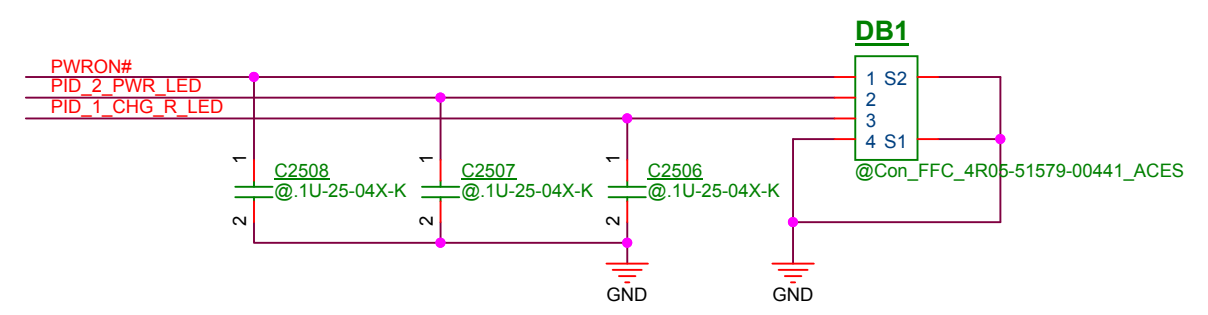
# Charge LED



# Touch Pad

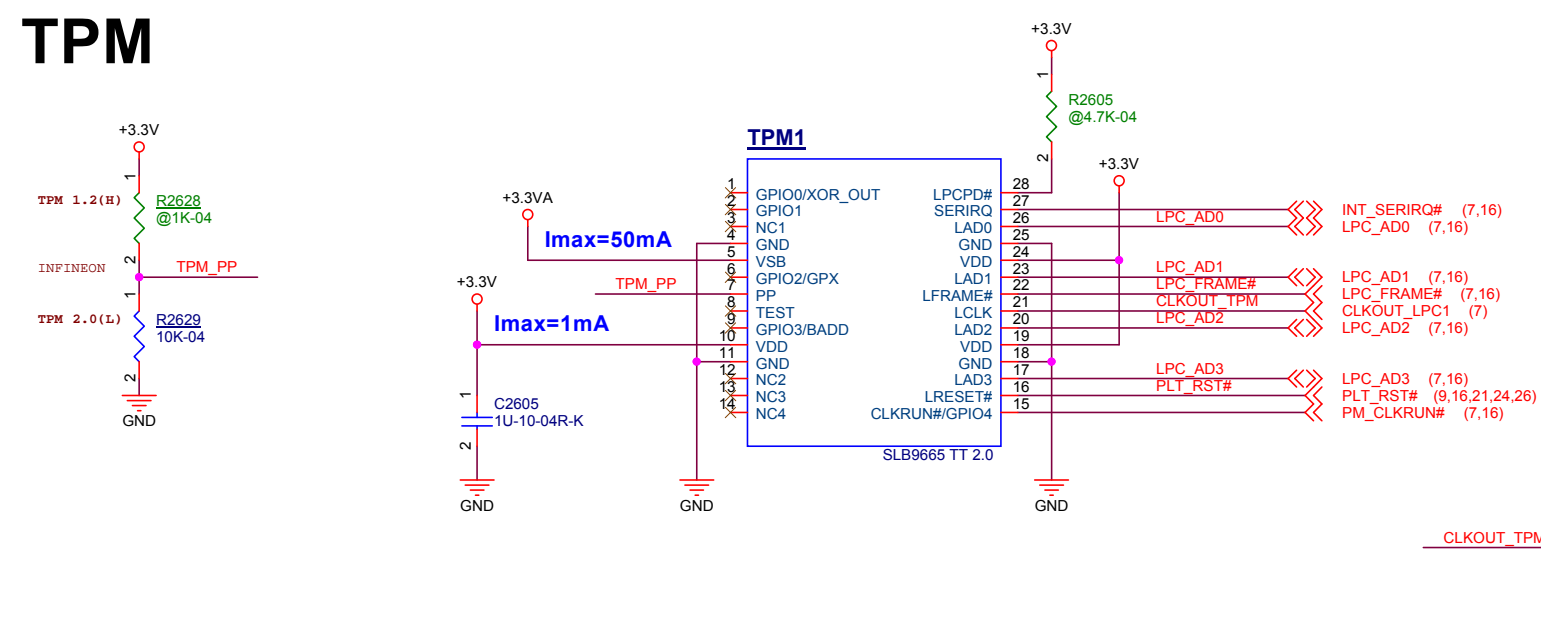


# PWR\_BD

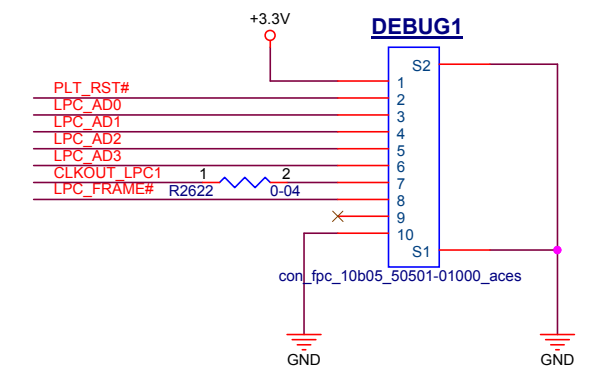


<b>Shuttle®</b>		<b>www.shuttle.com</b>	
<b>Title PWR SW/TP/CHG LED/PWR_BD</b>			
<b>Size B</b>	<b>Document Number NS4SL01</b>		<b>Rev A</b>
<b>Date:</b>	<b>Monday, November 23, 2015</b>	<b>Sheet 25 of 34</b>	

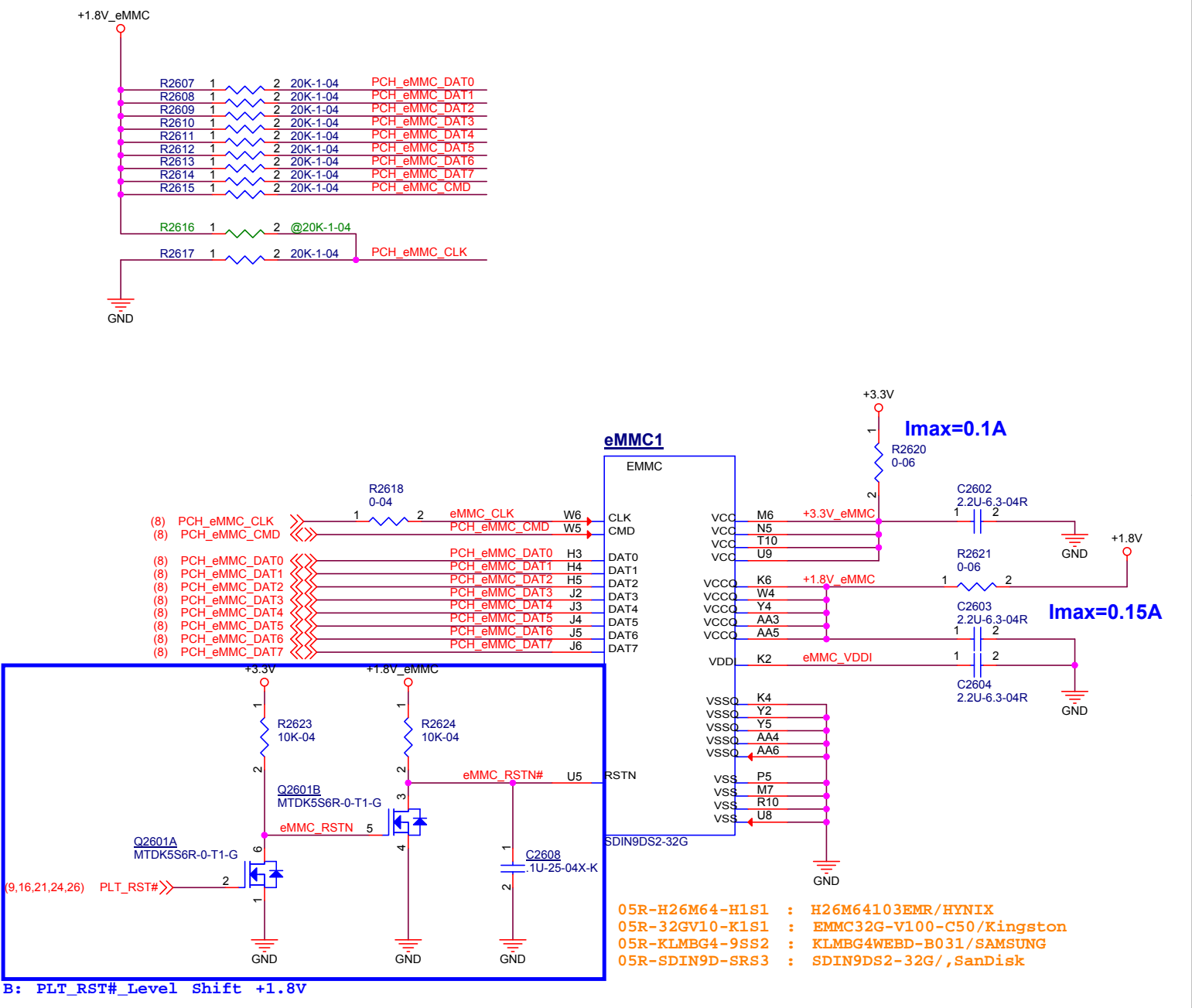
# TPM



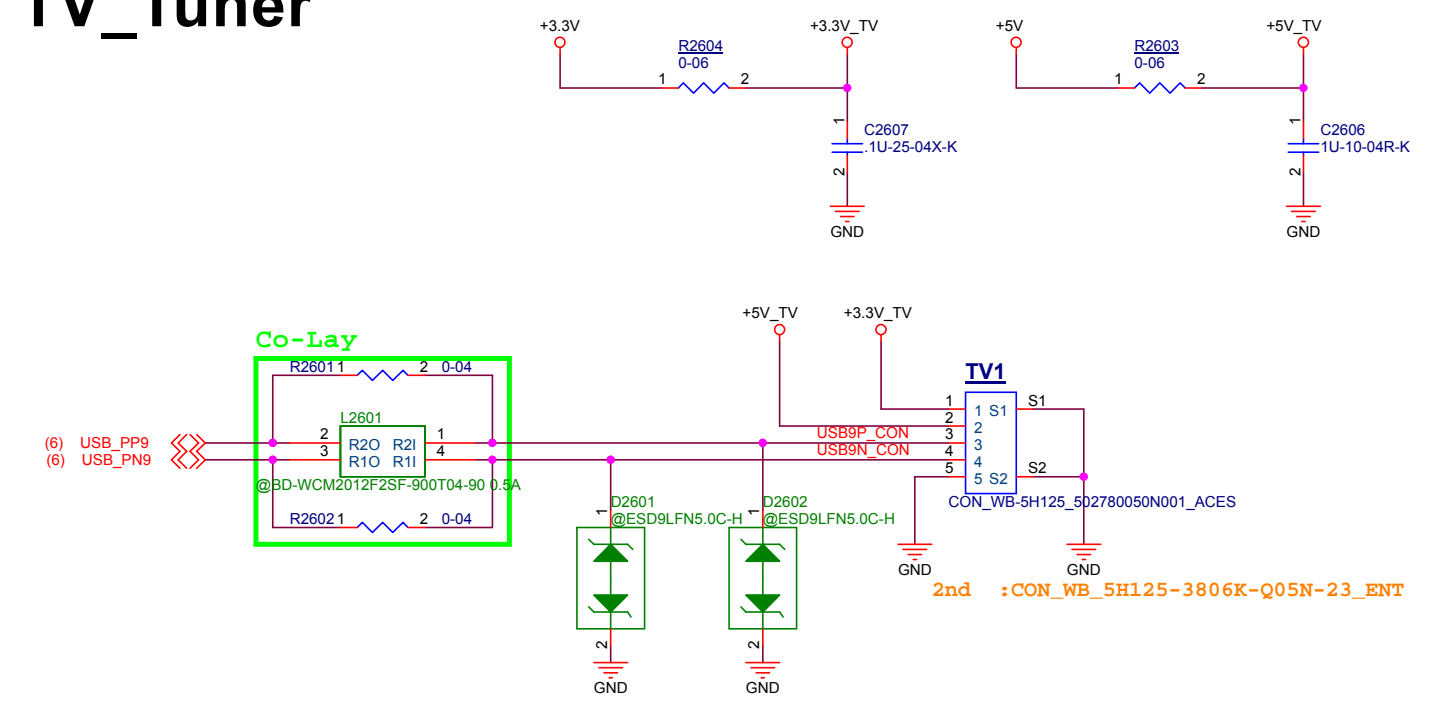
# DEBUG\_PORT



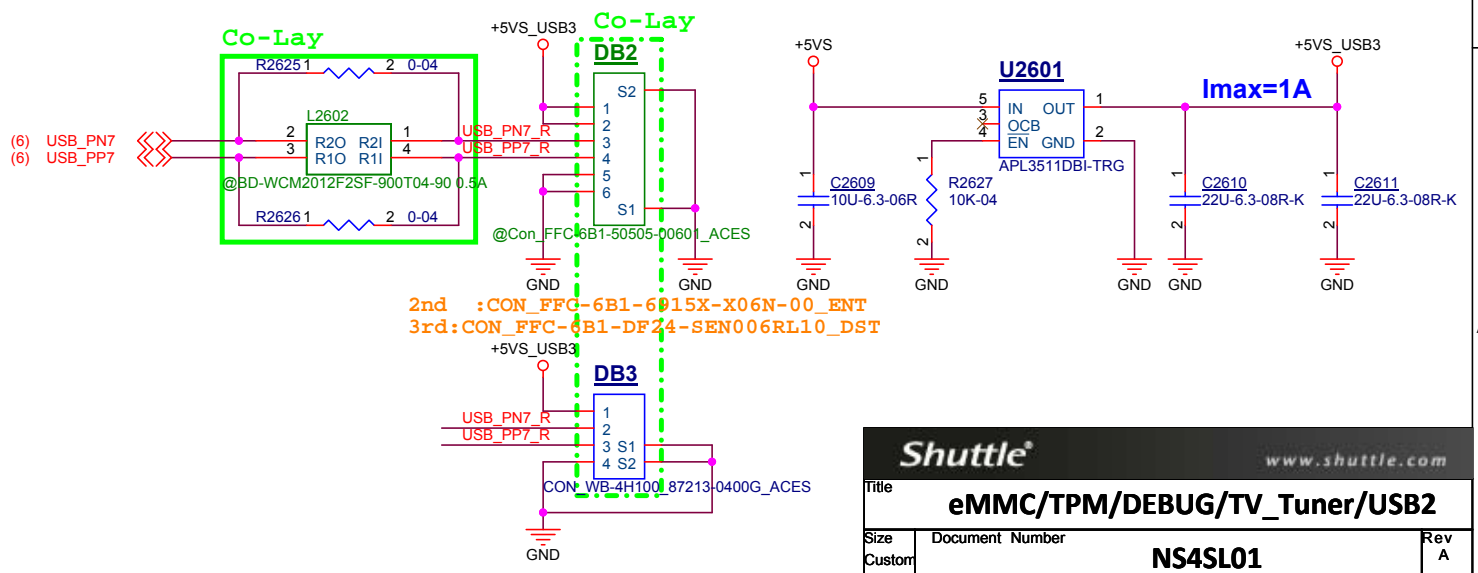
# eMMC

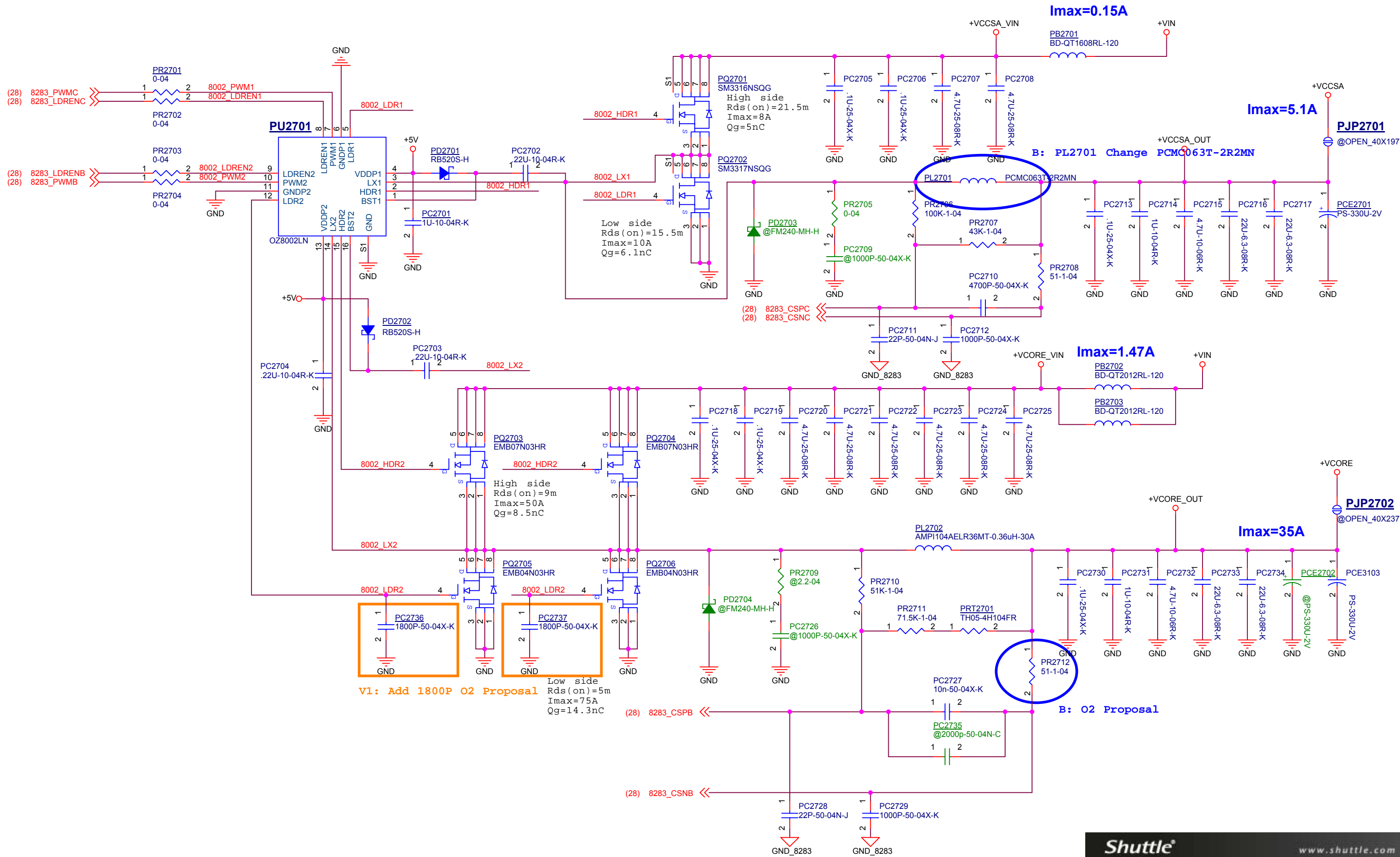


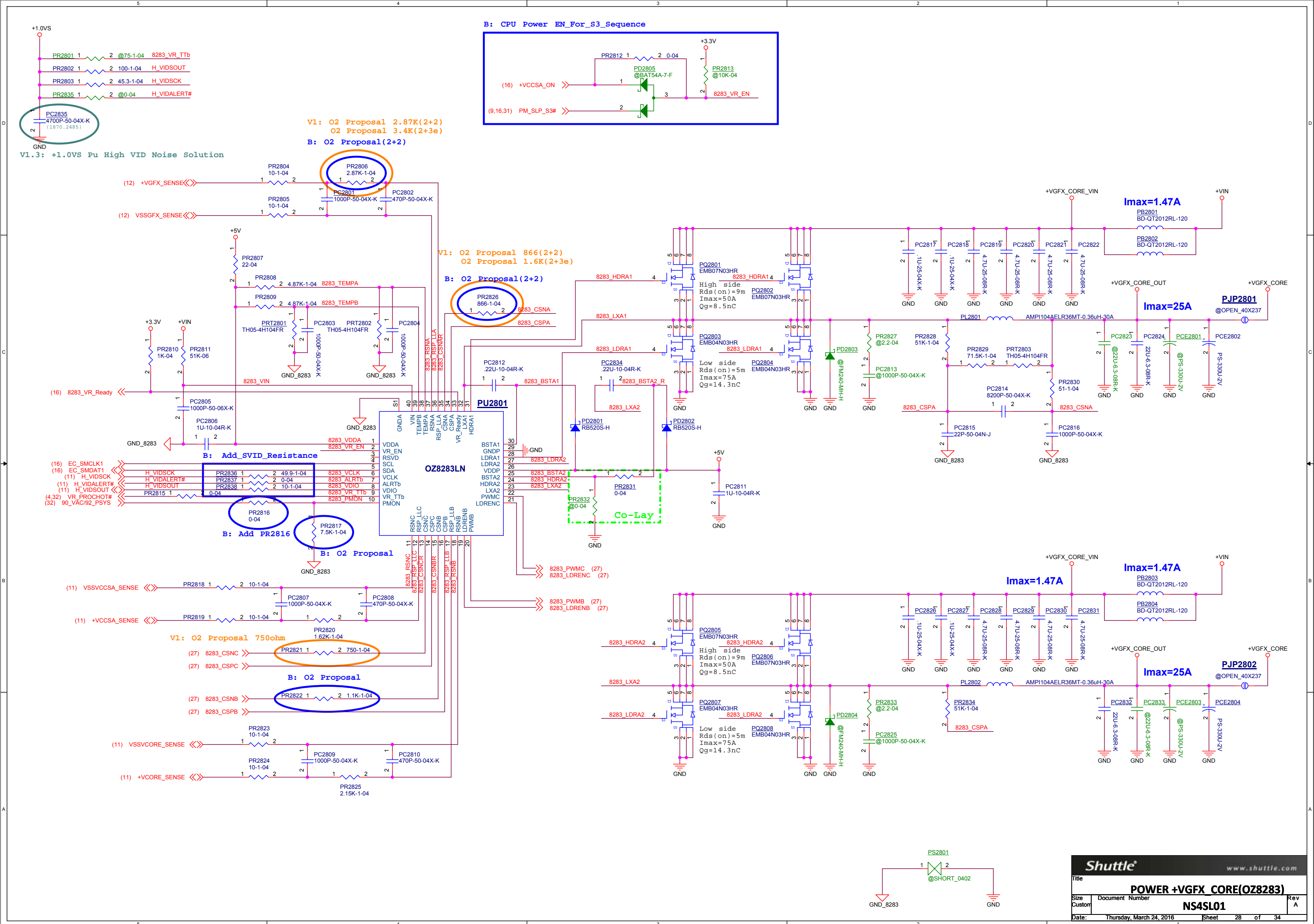
# TV\_Tuner



# USB2.0\_IO

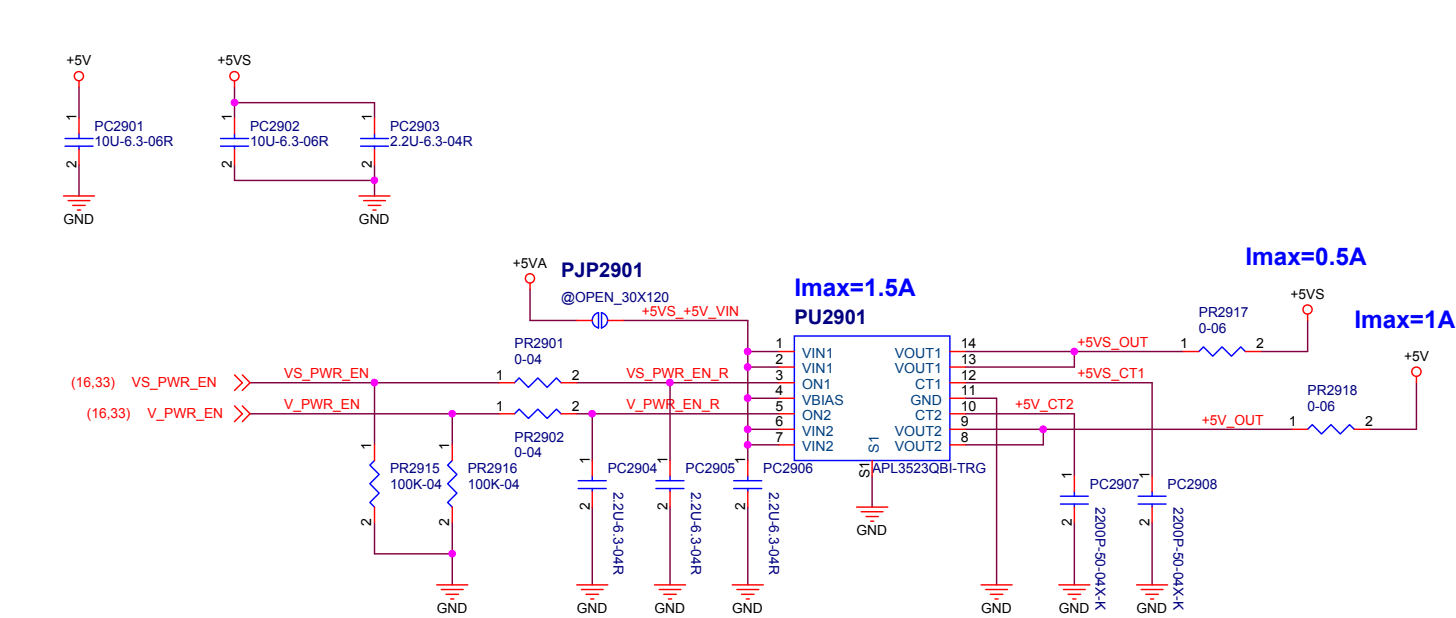




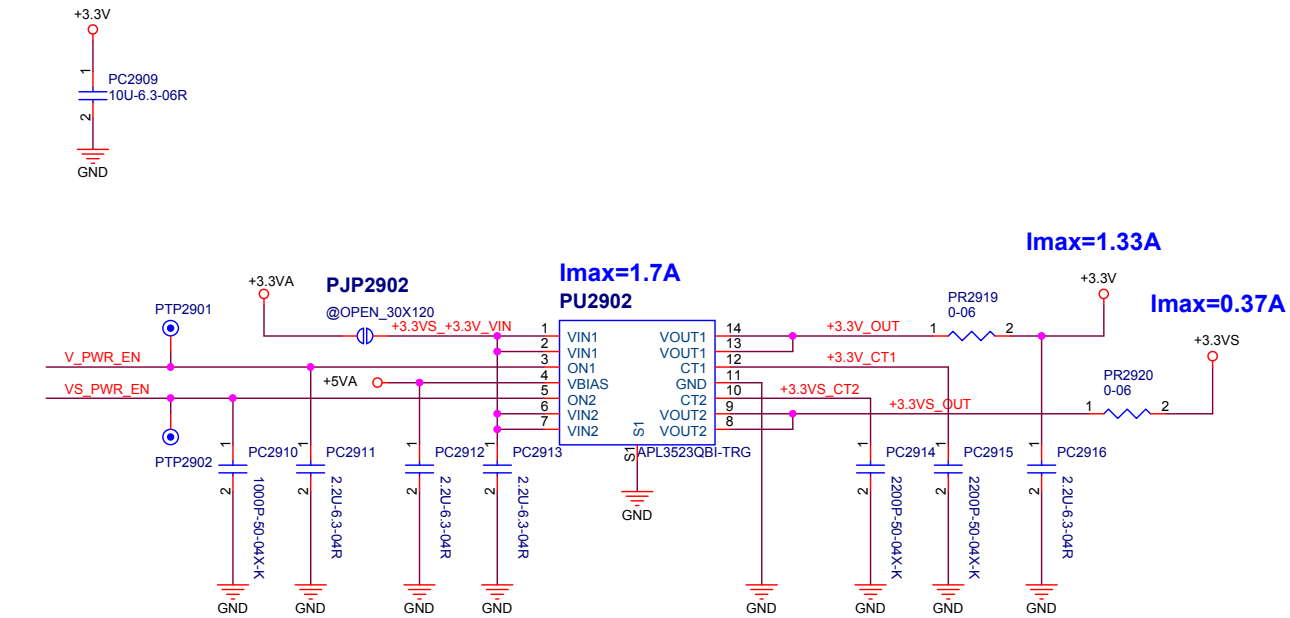




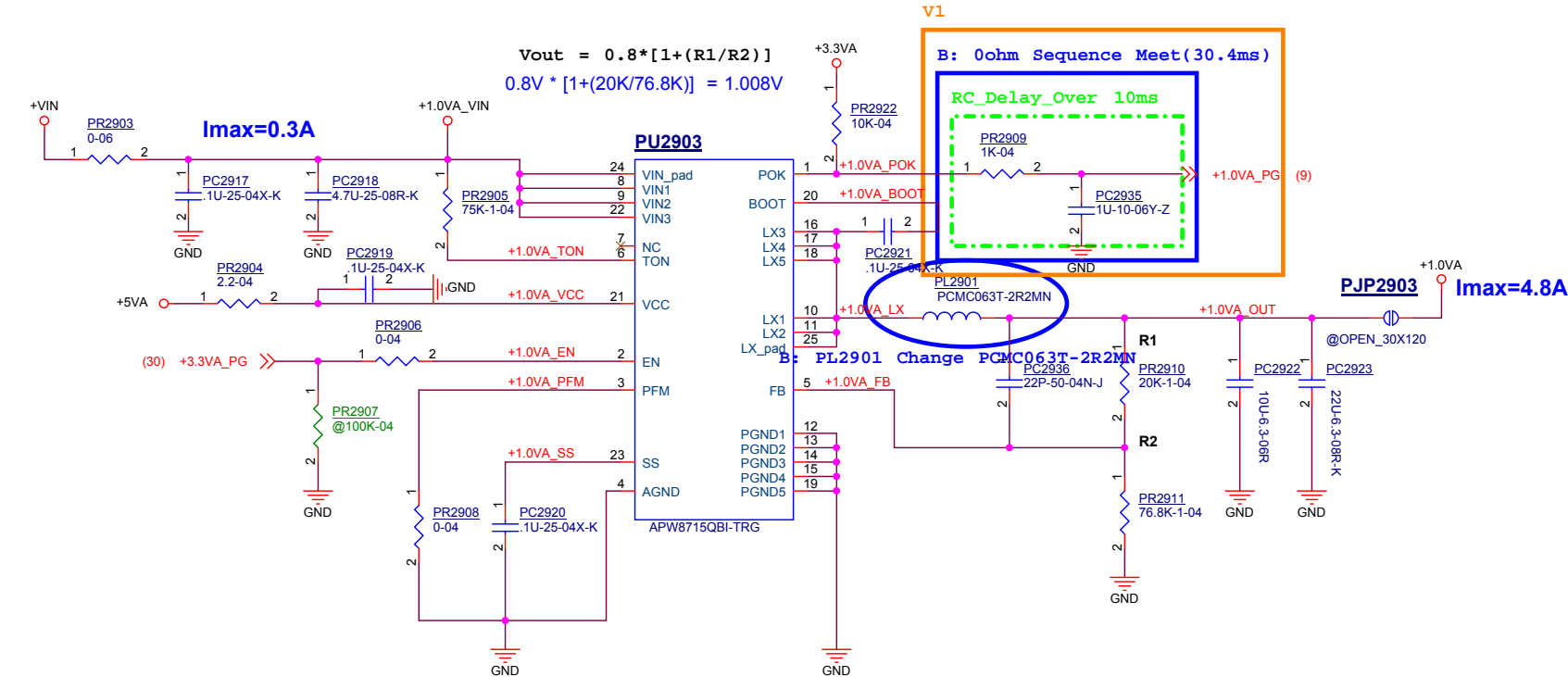
# +5VS/+5V Load Switch



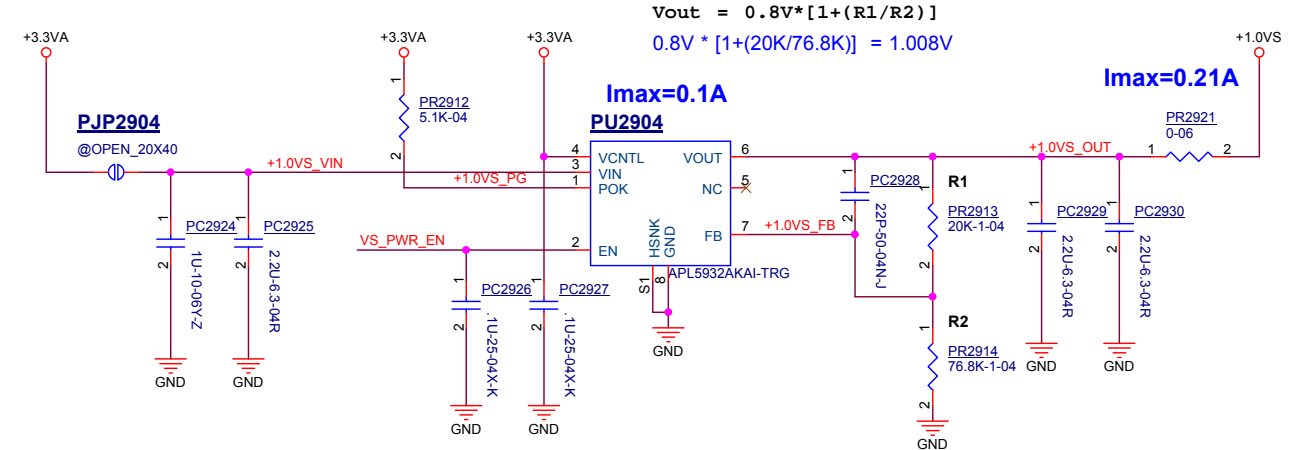
# +3.3VS/+3.3V Load Switch



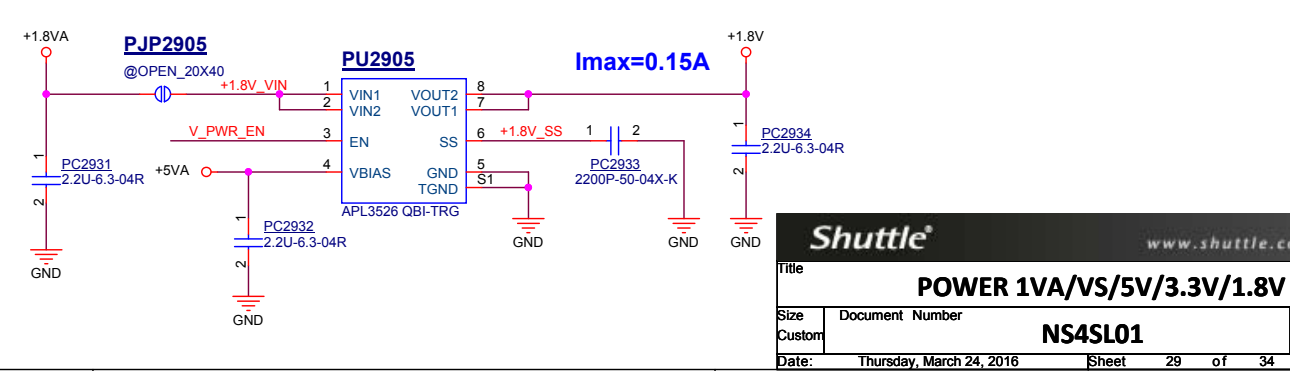
# +1.0VA Converter



# +1.0VS LDO

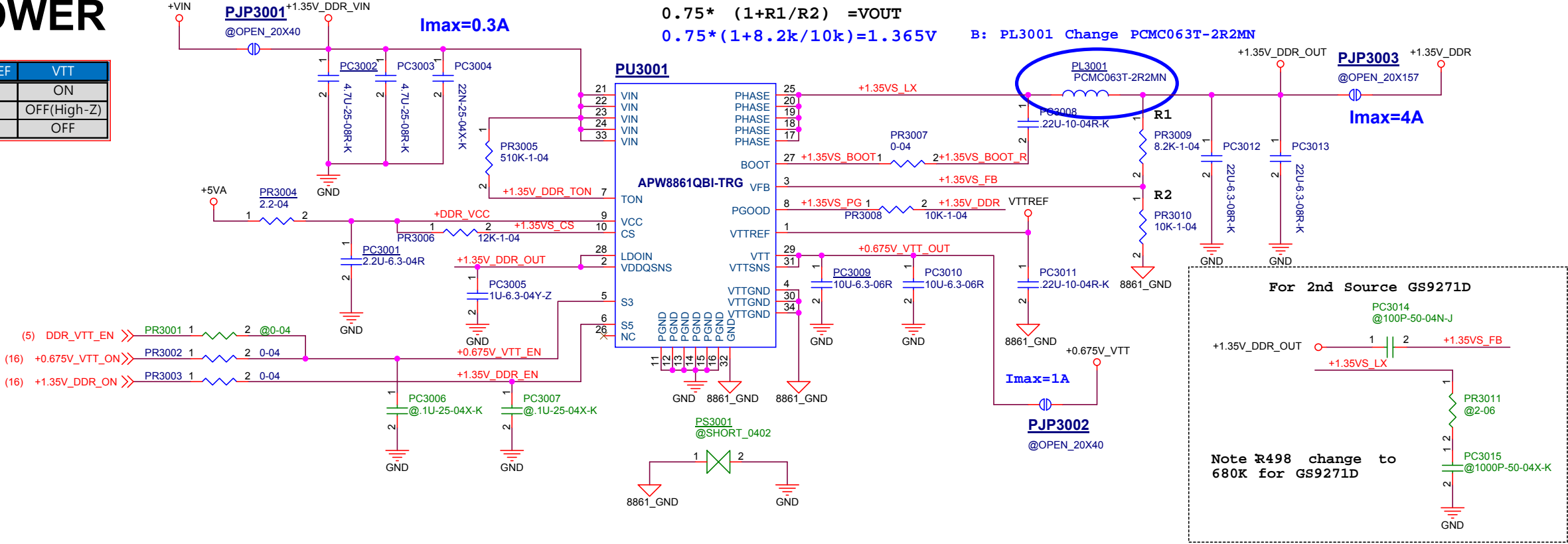


# +1.8V Load Switch

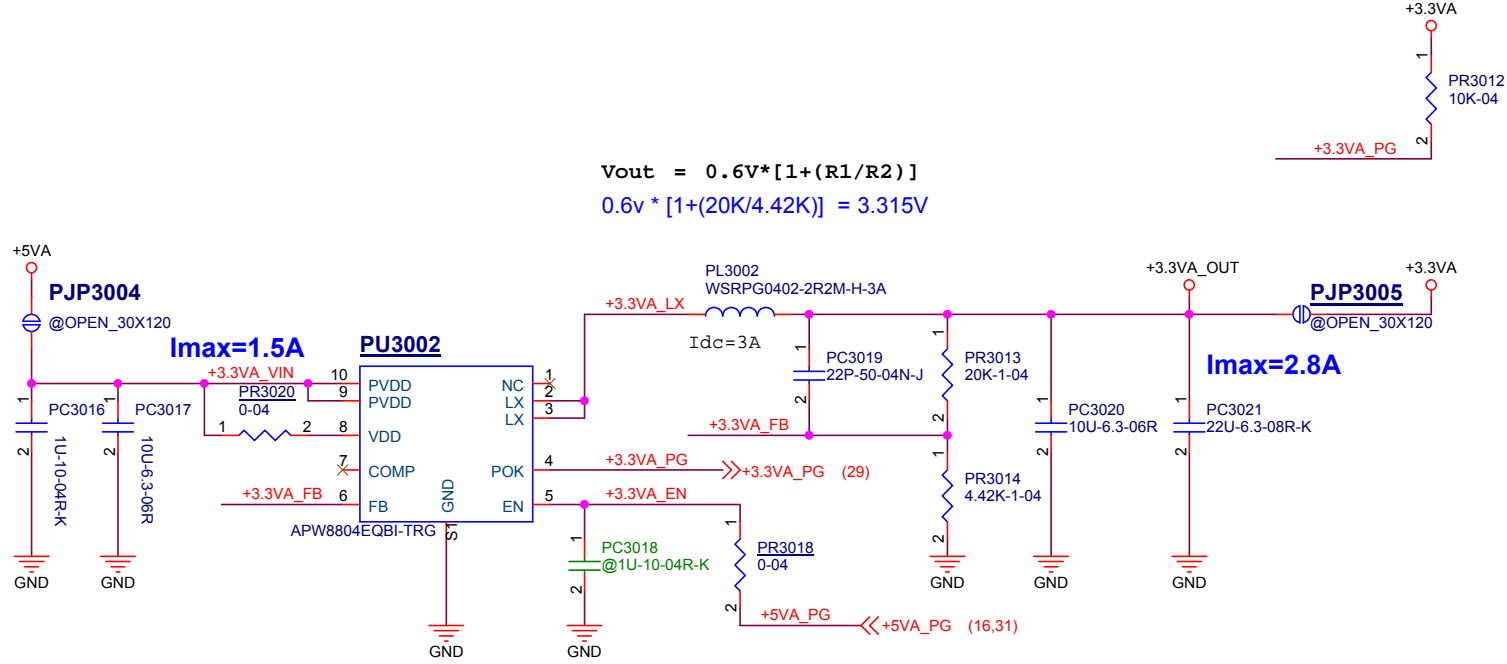


DDR3L POWER

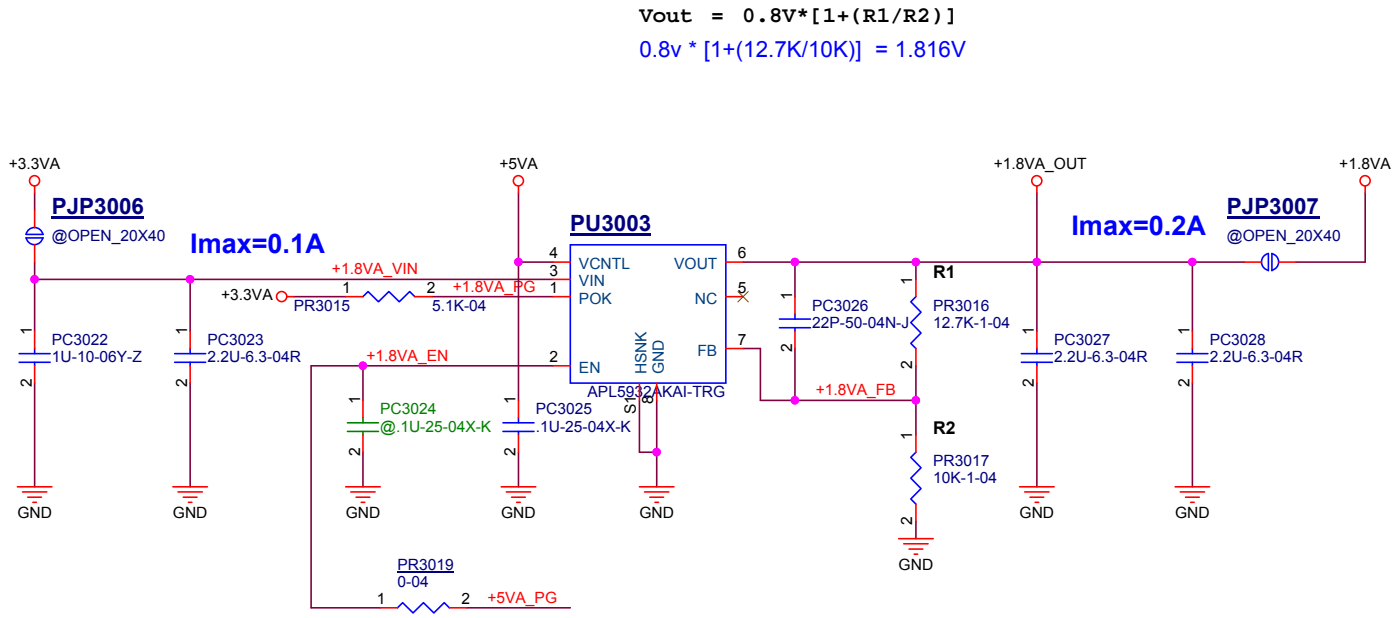
State	EN1	EN2	VDDQ	VTTREF	VTT
S0	High	High	ON	ON	ON
S3	Low	High	ON	ON	OFF(High-Z)
S4/S5	Low	Low	OFF	OFF	OFF



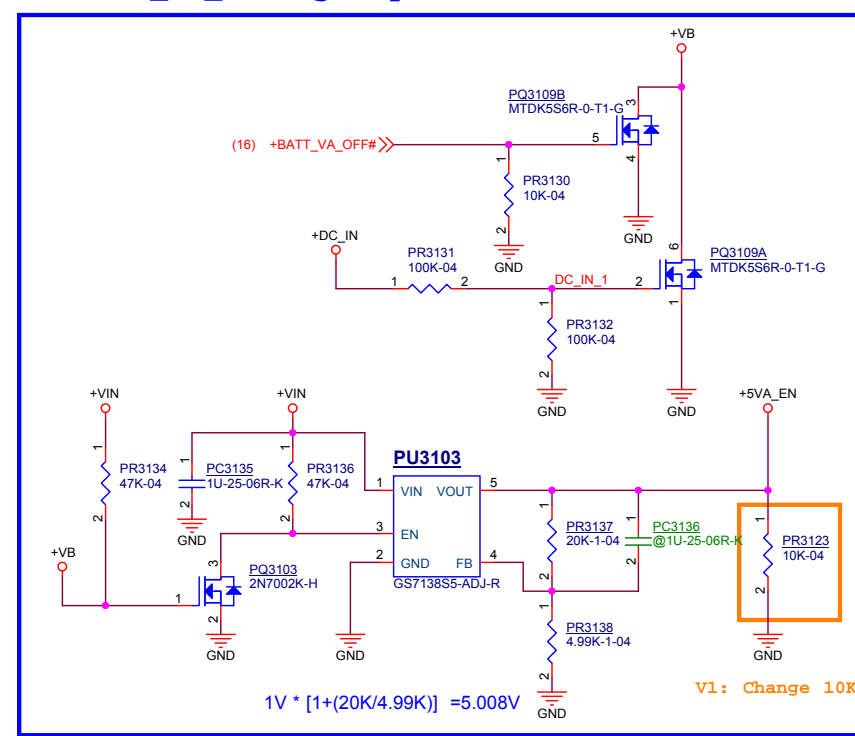
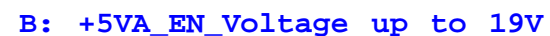
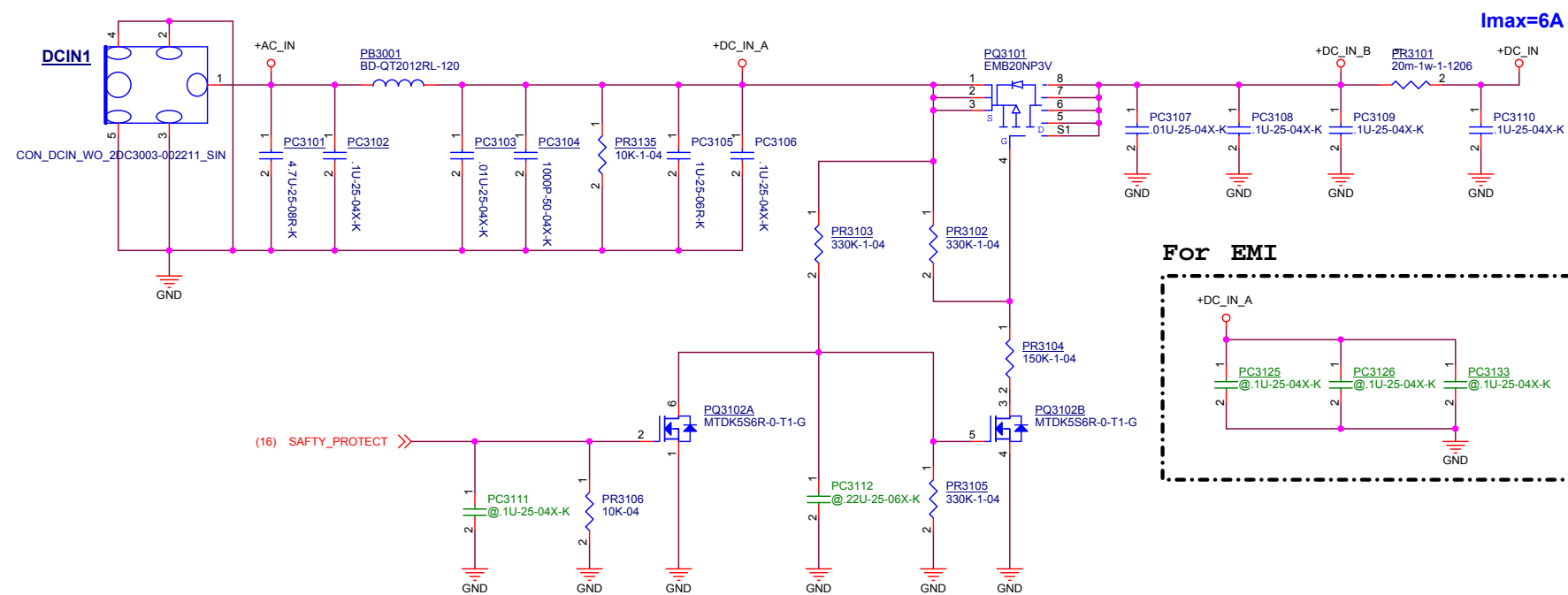
+3.3VA Convert



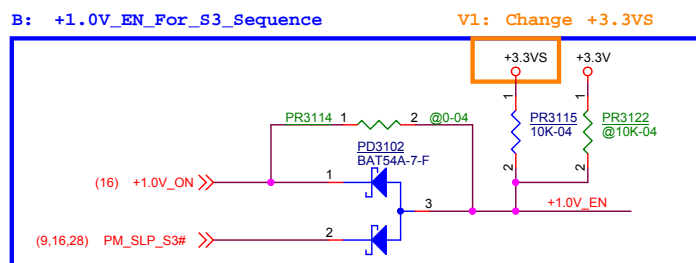
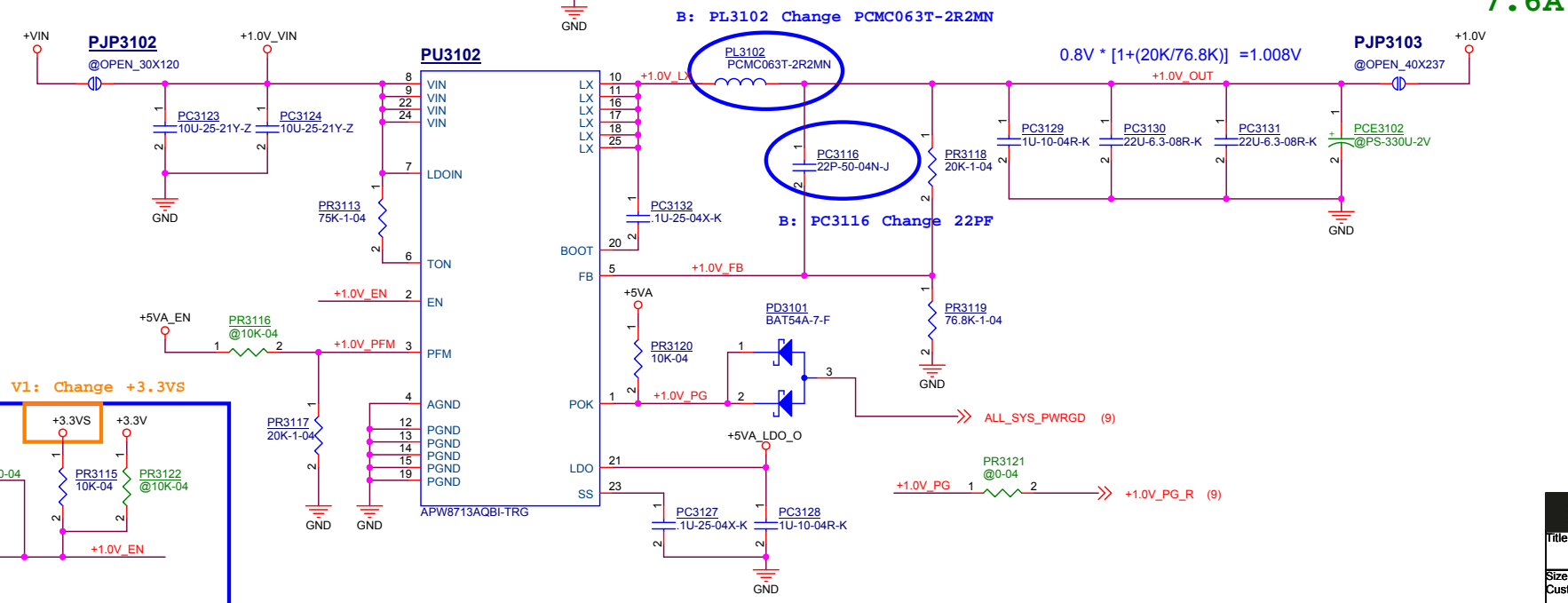
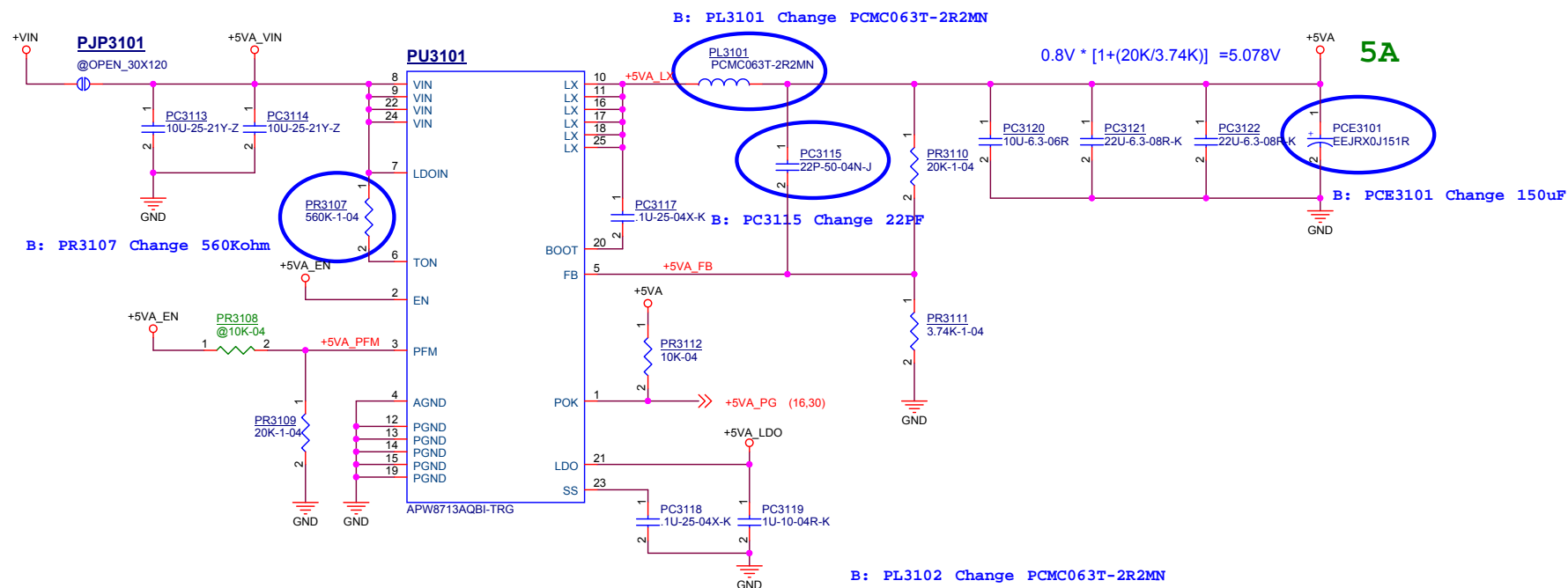
+1.8VA LDO



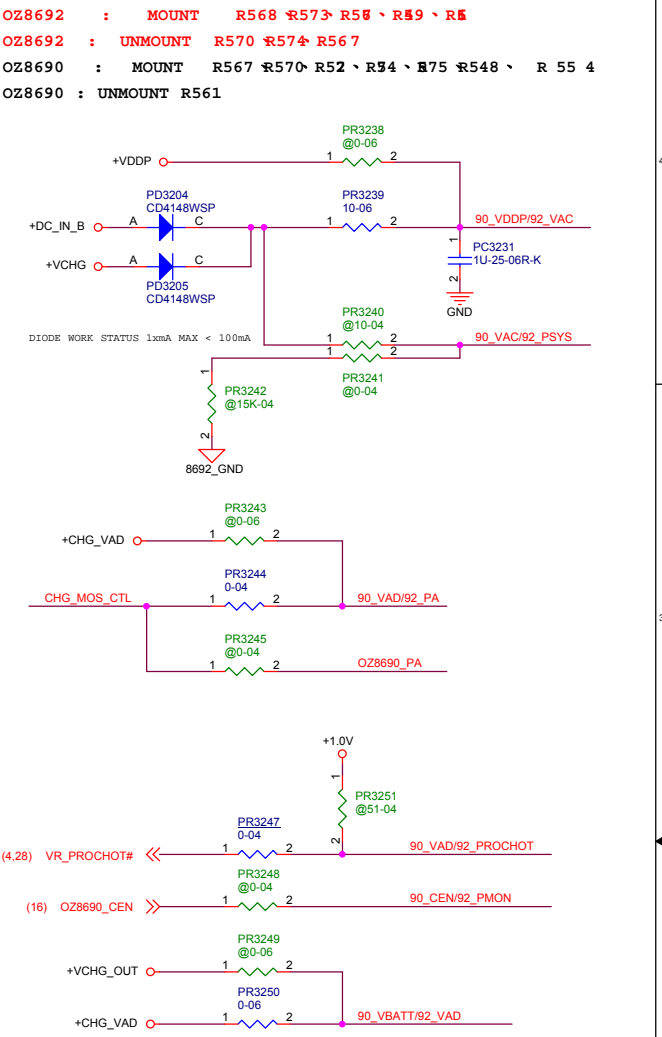
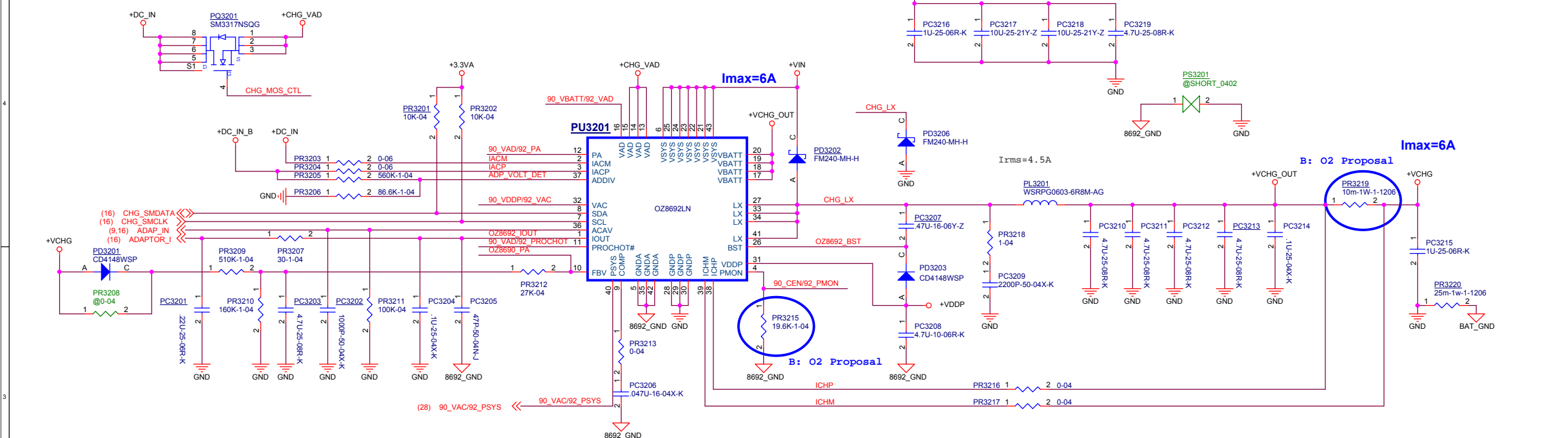
## DC IN



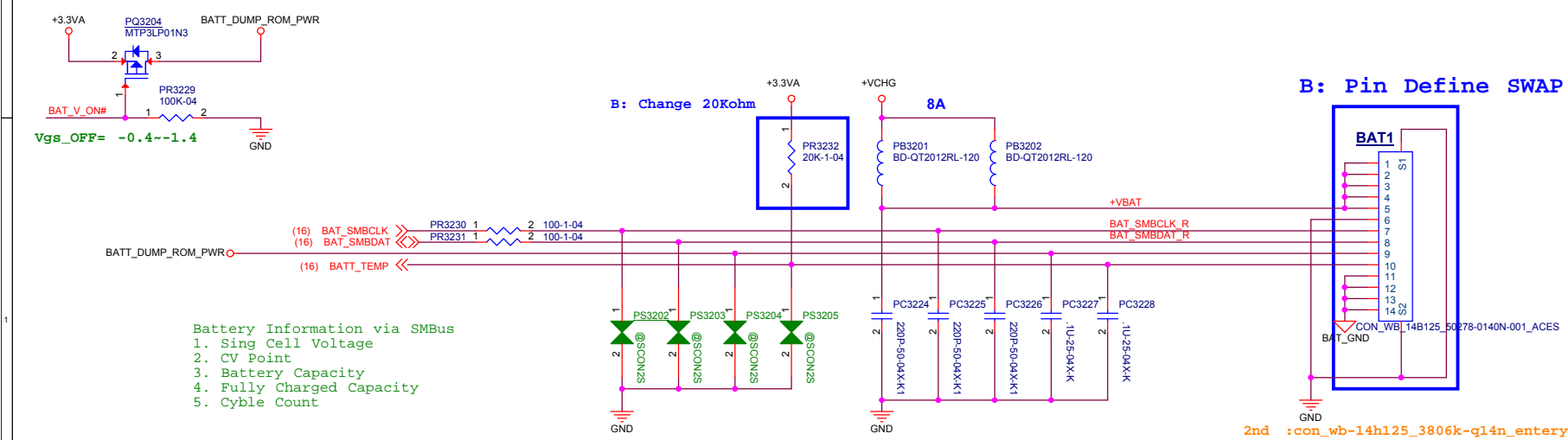
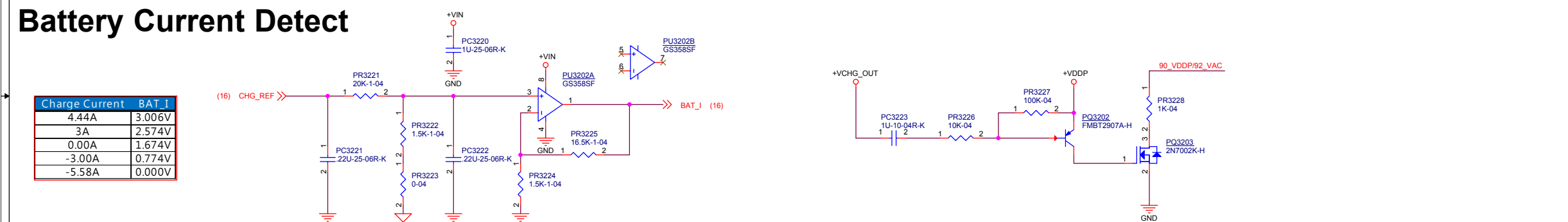
## +5VA/+1.0V



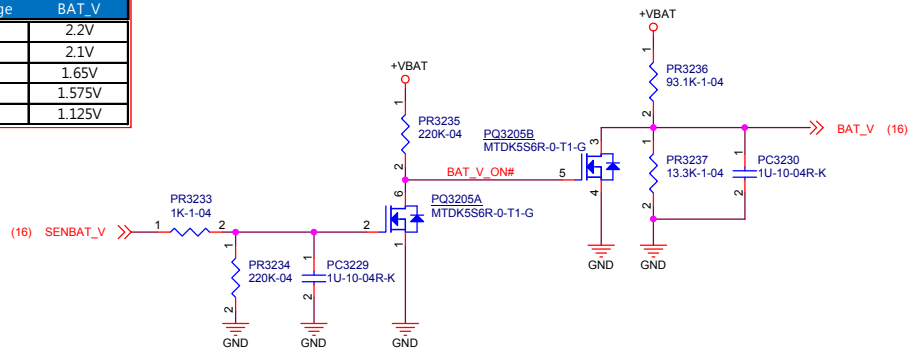
```
OZ8692      :      MOUNT      R568 R573 R568、R59、R5
OZ8692      :      UNMOUNT    R570 R574 R567
OZ8690      :      MOUNT      R567 R570 R52、R34、R75 R548、R 55 4
OZ8690      :      UNMOUNT    R561
```



## Battery Voltage Detect



BAT_Voltage	BAT_V
17.6V	2.2V
16.8V	2.1V
13.2V	1.65V
12.6V	1.575V
9.0V	1.125V



```
Battery Information via SMBus
1. Sing Cell Voltage
2. CV Point
3. Battery Capacity
4. Fully Charged Capacity
5. Cyble Count
```





B Phase Modify :

- 1.Add USB2.0 Port7 D/B(Page6)
- 2.Del R0716 For LPC(Page7)
- 3.VCCST\_PWRGD Change to +1.0V\_For\_Seq(Page9)
- 4.Del R0904 For ACPRESENT(Page9)
- 5.RTC1 Con Pin SWAP(Page9)
- 6.Add USB2.0 D/B(Page15)
- 7.Add PANEL\_DET0\_For Panel Size(Page16)
- 8.PM\_SLP\_S3# & PM\_SLP\_S4# Add 0ohm(Page16)
- 9.PM\_SLP\_S3# & PM\_SLP\_S4# Add 0.1uF Cap(Page16)
- 10.Change RTL8411BN(Page21)
- 11.M.2 Card Power Change +3.3VA(Page24)
- 12.Del R2418(Page24)
- 13.eMMC PLT\_RST#\_Level Shift to +1.8V(Page26)
- 14.Add USB2.0 D/B(Page26)
- 15.PR2712 51Kohm -> 51ohm(Page27)
- 16.PR2806 Modify 3.4Kohm(Page28)
- 17.PR2826 Modify 1.6Kohm(Page28)
- 18.PR2817 Modify 7.5Kohm(Page28)
- 19.PR2816 Add 0ohm(Page28)
- 20.PR2822 Modify 1.1Kohm(Page28)
- 21.PR2909 Modify 0ohm Meet DSW\_PWROK Sequence(Page29)
- 22.Del PU2902(Page29)
- 23.+5VA\_EN\_Voltage up to 19V(Page31)
- 24.PR3215 Modify 19.6Kohm(Page32)
- 25.PR3219 Modify 10mohm(Page32)
- 26.PR3232 Modify 20Kohm(Page32)
- 27.BAT Con SWAP(Page32)
- 28.Add\_U1801\_For Panel Pour Power(Page18)
- 29.CPU Power EN\_For\_S3\_Sequence(Page28)
- 30.+1.0V\_EN\_For\_S3\_Sequence(Page31)
- 31.Change 330uF POS CAP CE1101 & CE1102(Page11)
- 32.R2510 & R2511 Change 330ohm\_For LED Brightness(Page25)
- 33.Add C0908\_For VCCST\_PWRGD Sequence(Page9)
- 34.VCCSTG\_G20 Change +1.0V(Page11)
- 35.Add +VIN\_LCD\_DSG(Page17)
- 36.Vender Test Report C0901 & C0902 Change 15PF(Page09)
- 37.PL2701 Change PCMC063T-2R2MN(Page27)
- 38.PR3107 Change 560Kohm(Page31)
- 39.PL3101 & PL3102 Change PCMC063T-2R2MN(Page31)
- 40.PC3115 & PC3116 Change 22PF(Page31)
- 41.PCE3101 Change 150uF(Page31)
- 42.PL2901 Change PCMC063T-2R2MN(Page29)
- 43.PL3001 Change PCMC063T-2R2MN(Page30)
- 44.+0.675\_VTT Change 22uF Cap(Page14)
- 45.THERMTRIP# Pu Up Change 1.0VS(Page04)
- 46.PROC\_SELECT# Pu Up 100K Change 1.0VS(Page10)
- 47.Add LAN WAKE & CLKREQ Switch Solution(Page21)
- 48.Add WLAN WAKE & CLKREQ Switch Solution(Page24)
- 49:R0923 Change 1Mohm(Page49)
- 50.Add R1005 Pu Up +3.3VA For NS4SL01 BIOS Verb Table(Page10)
- 51.Change 330uF POS CAP(Page12)



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